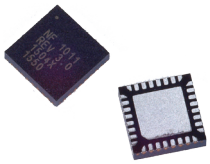
DATA SHEET

NF1011
Frequency Translator and Jitter Attenuator

Overview



The NF1011 is a high performance frequency translator and jitter attenuator which is designed to meet requirements for multiple applications where low phase noise and ultra low jitter outputs are required including: frequency translation supporting wireless communication, 40G,100G and 400G Synchronous Ethernet, Sonet, OTN and IEEE 1588 network elements, clock translation with low phase noise, and other applications demanding sub-picosecond jitter performance.

The NF1011 consists of a PLL stage that attenuates the jitter of the reference input with the use of an integrated phase detector, charge pump and external VCXO. The NF1011 generates a single-ended LVCMOS clock output channel based on the frequency of the external VCXO.

The NF1011 accepts one reference input. The REF input can accept a single-ended LVCMOS clock signal. The LVCMOS input can take any frequency from 8KHz to 160MHz.The NF1011 is supported by an external LVCMOS VCXO from 10MHz to 160MHz.

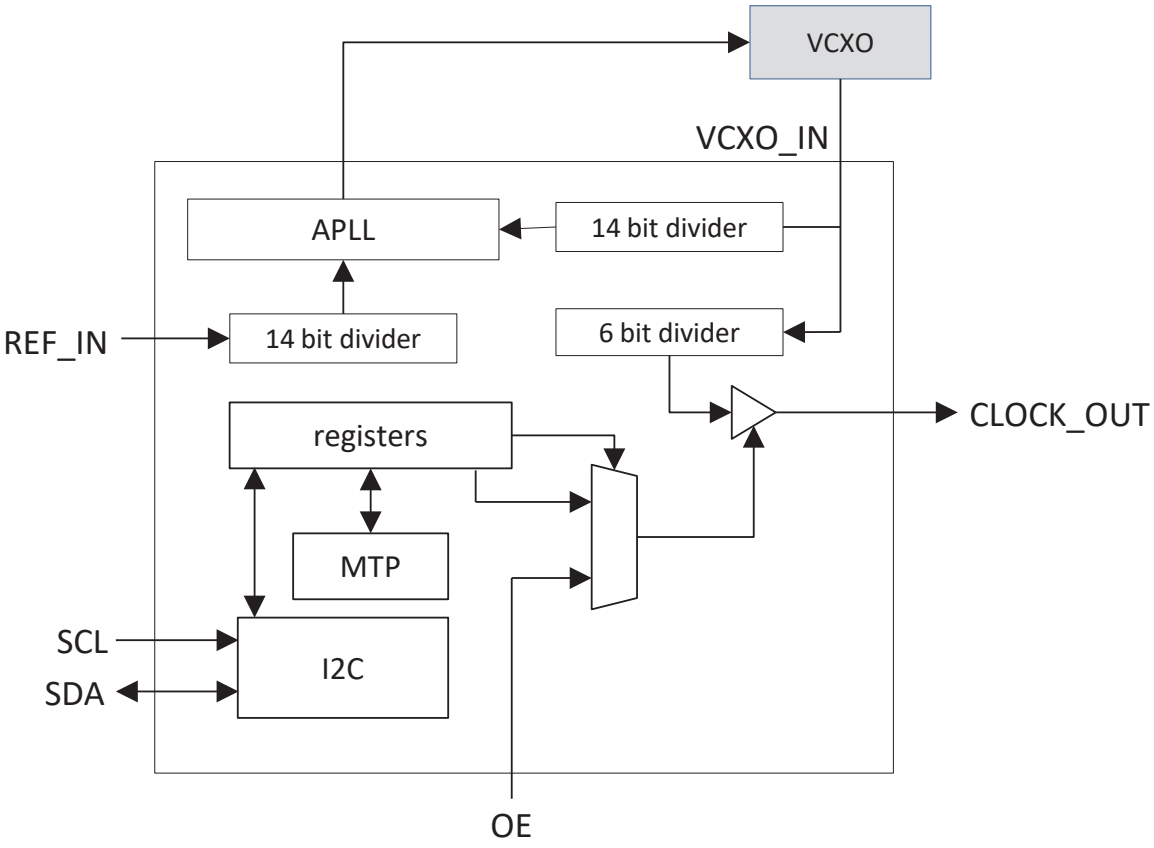
Features

- Simple operation accepts one reference input and generates one output channel.
- Reference input accepts one single-ended 3.3V LVCMOS clock signal from 8 kHz up to 160 MHz.
- Generates one output channel based on the frequency of the external VCXO which drives one single-ended L VCMOS output with 6 bit divider circuit at Output transmitter.
- Accepts 3.3V LVCMOS VCXO input at frequencies from 10MHz to 160MHz.
- Internal multiple time programmable (MTP) memory bank.
- Programmable phase detector rate of PLL is minimum 8kHz to 500 KHz.
- Capable of <60fs jitter performance over 12kHz to 20MHz integration.
- Programmable Charge Pump current.
- Minimal external components required due to internal charge pump Caps.
- Supports I2C bus interface.
- Operating temperature range of -40°C to 85°C.
- 3.3V operation.
- 40-pin QFN package (5mm x 5mm)

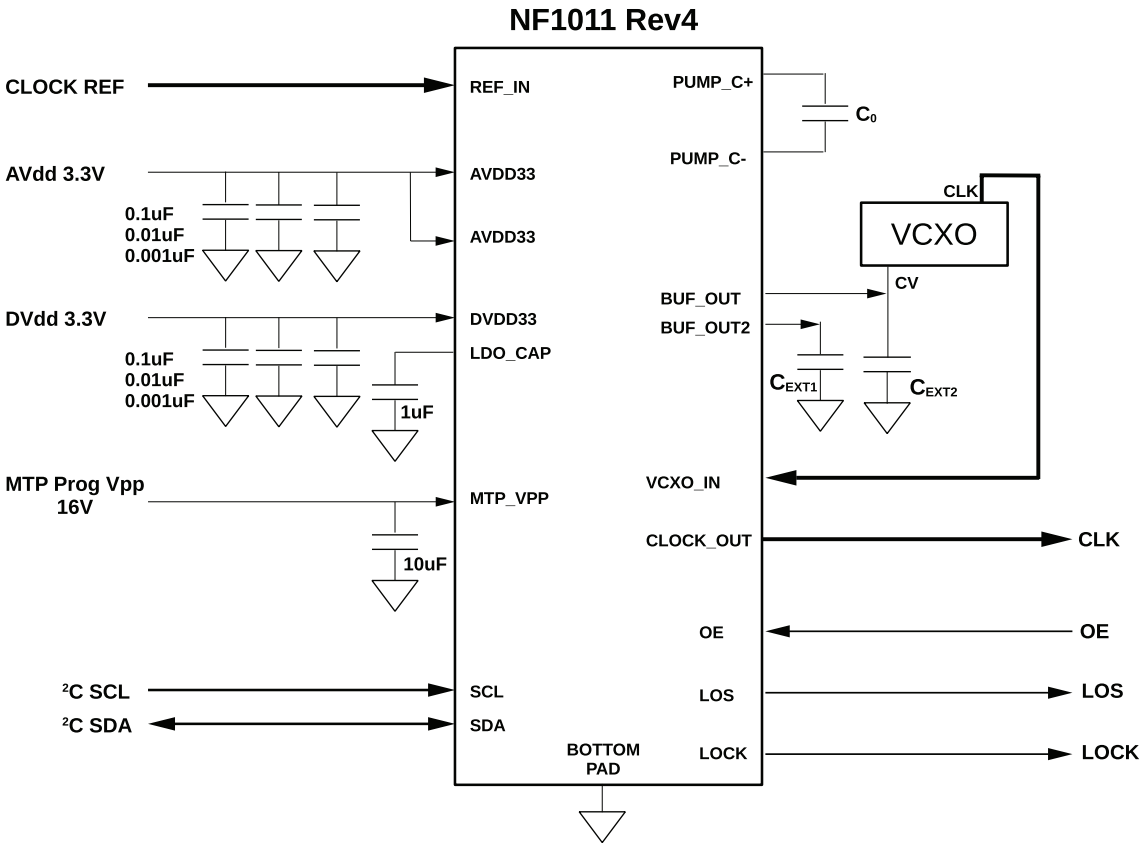
Applications

- High Stability Clocking
- Primary Reference Time Clock (PRTC) [G.8272]
- Telecom Grand Master [G.8273.1]
- Telecom boundary clock [G.8273.2]
- Wireless Base Stations
- GNSS Disciplined Oscillator
- NTP Stratum 0 Standard

NF1011 Functional Block Diagram



Typical Application



General Description

The NF1011 is a frequency translator and jitter attenuator. Fundamentally, the input PLL consists of a phase-frequency detector (PFD), charge pump, passive loop filter, and an external VCXO operating in a closed loop. The NF1011 PLL has the flexibility to operate with a loop bandwidth of approximately 10Hz to 200 Hz. This relatively narrow loop bandwidth gives the NF1011 the ability to suppress jitter that appears on the input reference. The output of the PLL then becomes a low jitter phase-locked version of the reference input system clock.

The charge pump current is programmable in the NF1011. An external capacitor is required for the NF1011's loop filter. Typically, this loop filter may operate at 100Hz when a 0.22uF capacitor is connected.

The NF1011 is capable of attenuating the jitter of the reference input with approximately 40fs additive jitter to that of the external 3.3V VCXO system clock when properly configured and a design implementation incorporating low noise PCB layout techniques.

Reference Inputs

The NF1011 accepts one reference input source. The incoming reference input is single-ended mode (LVCMOS) supporting frequencies from 8KHz up to 160MHz.

PLL Input Dividers

The reference input feeds a dedicated reference divider block. The input divider provides division of the reference in integer. The size of the divider for single ended inputs is 14 bit. The divider provides the bulk of the frequency pre-scaling that is necessary to reduce the reference frequency to accommodate the bandwidth that is typically desired for the PLL.

Phase Frequency Detector

The phase frequency detector range of the NF1011 is 8KHz to 500KHz.

Charge Pump

The NF1011 charge pump current is programmable in a range of 0 to 1280uA.

PLL Loop Filter

The PLL loop filter requires the connection of an external capacitor between pins PUMP_C+ (pin 2) and PUMP_C- (pin 1). The value of the external capacitor depends upon the characteristics of the VCXO, as well as such configuration parameters as input clock rate and desired bandwidth.

An external filter can also be used at the BUF_OUT (pin 4) and BUF_OUT_2 (pin 3) optionally. This R-C network filters the noise associated with the VCXO voltage control pin to achieve the best phase noise performance.

Clock Output

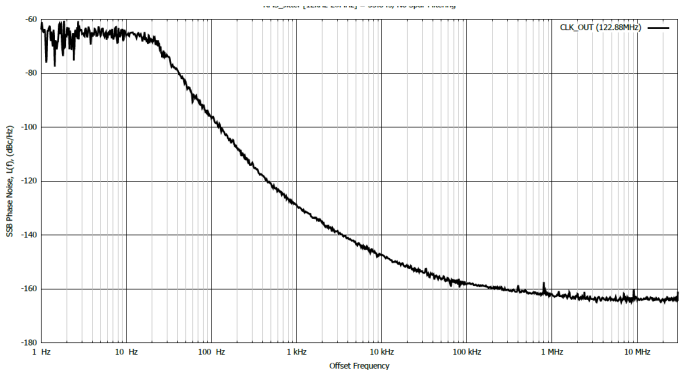
The NF1011 supports a single ended VCXO into pin 7 (VCXO_IN). The output clock is generated on Pin 8 (CLOCK_OUT) at the same frequency of the VCXO. A 6 bit divider circuit is available at the output that can be used to divide the output from the VCXO frequency up to a value of 63.

Clock Outputs continued

The frequency range of the LVCMOS clock output is from 10 MHz to 160 MHz, divisible with the 6 bit divider circuit from the VCXO frequency. The output RMS jitter performance of the NF1011 is determined by the jitter performance of the external VCXO used but is capable of < .05 picosecond level over integration range from 12kHz to 20MHz.

Optimizing spurs may involve some trial and error. Phase detector spurs occur at an offset from the carrier equal to the phase detector frequency. In some cases where the loop bandwidth is very wide relative to the phase detector frequency, some benefit might be gained from using a narrower loop bandwidth. Bypassing at the supply pins and board layout can also have an impact on this spur, especially at higher phase detector frequencies.

122.88MHz LVCMOS Output (locked to 10MHz TXCO REF input)



Lock Status and Loss of Signal Alarm

Lock (LOCK) and Loss of Signal (LOS) are detected and two pins 22 and 23 are available to indicate whether the PLL is in lock or if a loss of signal has occurred.

Pin LOCK indicates when the PLL is locked to the incoming reference. Alarm pin, LOS, indicates loss of signal on the reference input.

Output Enable

The output enable function is controlled by how register 0x0a is set. Setting "0" to 0x0a will disable the output unless a non zero number is used in the post divider setting register 0x09. A setting of "1" to this register activates pin 28 to be hardware controllable with Enable "on" when Pin 28 is HIGH and disable "off" when Pin 28 is LOW.

NF1011 Power Requirements

The NF1011 requires a 3.3V digital power input (DVDD33) to pin 25. 3.3V power supply is needed for analog power input (AVDD33) to pin 6 and pin 10. For MTP programming, 6.5V is required at pin 21 (MTP_VPP) during programming.

Multiple Time Programming (MTP) Memory

The NF1011 has internal memory that allows the internal register settings to be stored and loaded each time the IC is powered up.

1. Apply 6.5V to pin 21 MTP_VPP
2. Set Nearest VCXO to 10kHz Divider Value register
3. Write 0x77 to register 0x15
4. When register 0x15 becomes to 1, the burn is complete

The NF1011 has internal memory that allows the NF1011 register settings to be stored internally and loaded each time the IC is powered up. To enable programming to this memory bank, a +6.5V supply must be applied at pin 21 (MTP_VPP) during the burn process. This memory bank can be programmed up to 255 times. Each time the memory is burned with valid content, the IC will start up entering those register settings. To provide the IC with an internal clock to support the programming process the VCXO clock signal is used, Register 0x18 ~ 0x19 is used to divide the VCXO frequency within a range of 10 kHz. A value must be determined and set in this register for programming to take place. If a calculated value is not an integer, the closest truncated integer should be chosen and entered into the register to achieve dividing as close to10kHz as possible.

When the MTP load status is complete and the number of MTP burned is less than 255, the following procedure can be used to burn the settings for registers 0x07 ~ 0x15 to the internal memory.

1. Set register 0x18~19,Nearest VCXO to 10kHz Divider Value, with an appropriate value
2. Apply 6.5V to MTP_VPP pin 21
3. Write 0x77 to register 0x15
4. When register 0x15 reads "1", the burn has been completed successfully.

PLL General Description

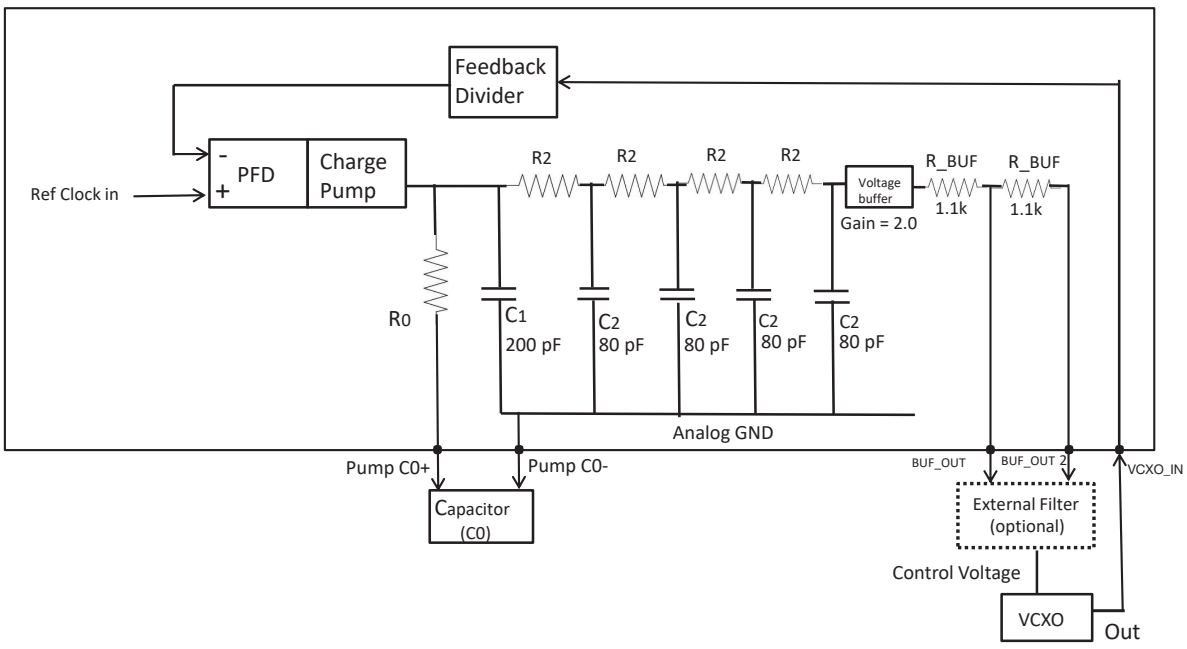
The NF1011 consists of a phase-frequency detector (PFD), charge pump, passive loop filter, and an external VCXO operating in a closed loop. The APLL is designed to operate with a loop bandwidth of approximately 10Hz to 200 Hz. The charge pump current ,feedback divider, R0,and R2 are register programmable inside the chip. Capacitors C1 and C2 are internal and are fixed values.

One external capacitor is required for the NF1011's loop filter, which connects to pins Pump_C0+ and Pump_C0-. An additional external filter optionally can be used on the control voltage pin of the external VCXO and is supported through BUF_OUT and BUF_OUT2 pins.

PLL Circuit Description

- Architecture: PD+CP+FILTER+ISO
- PD (phase detector): PFD
- Dividers: Two integer dividers, one on the reference clock and one on the feedback VCXO clock before feeding into the phase detector.
- CP (charge pump): current programmable.
- Filter: C0 External, connect to pin PUMP_C
- Filter: R0 (internal, programmable)
- Filter: C1 (internal, 200pf)
- Filter: R2 x4 internal R and x4 internal C cascaded as a distributed R/C. R (internal, programmable, all with same resistance you could program), C (internal, fixed, each one is 80pF).
- Impedance Isolator: a voltage buffer after the filter, with gain of x 2.0.
- This impedance isolator buffer drives into two internal resistors (in serial). Each of them has 1k ohm resistance.
- The end of the 1st resistor of the two post-buffer resistors has been tapped to pin 4
- The end of the 2nd resistor of the two post-buffer resistors has been connected to pin 3.

APLL Circuit Diagram



NF1011 Register Table

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x00 ~ 0x05	Chip ID	R	6 ASCII Code	NF1011	ASCII Code to represent chip ID
0x06	Chip Revision	R	[7:0]	4	Chip revision
0x07 ~ 0x08	VCXO to PFD Divider Value	RW	[13:0]	0	VCXO FREQ to PFD Feedback divider value
0x09 V	CXO to Output Divider Value	RW	[5:0]	1	VCXO FREQ to output FREQ post divider value
0x0a	Output Enable Source	RW	[0:0]	0	VCXO output enable control source, 0: based on VCXO output divider value, 0: disable, else enable 1: from external enable pin
0x0b ~ 0x0c	Reference to PFD Divider Value	RW	[13:0]	0	Reference FREQ to PFD FREQ pre-divider value
0x0d	R0 Range Selection	RW	[0:0]	0	0: use R0 Range_L, 80k ~ 5110k 1: use R0 Range_S, 10k ~ 77.5k (in ohms)
0x0e	R0 Range_S	RW	[4:0]	0	Bit[0]: 0/1: 0.4K/2.5K Bit[1]: 0/1: 0.4K/5K Bit[2]: 0/1: 0.4K/10K Bit[3]: 0/1: 0.4K/20K Bit[4]: 0/1: 0.4K/40K Total R value is the sum of all R value (in ohms)
0x0f ~ 0x10	R0 Range_L	RW	[8:0]	0	Bit[0] : 0/1: 1K/10K Bit[1] : 0/1: 1K/20K Bit[2] : 0/1: 1K/40K Bit[3] : 0/1: 1K/80K Bit[4] : 0/1: 1K/160K Bit[5] : 0/1: 1K/320K Bit[6] : 0/1: 1K/640K Bit[7] : 0/1: 1K/1280K Bit[8] : 0/1: 1K/2560K Total R value is the sum of all R value (in ohms)
0x11	R2	RW	[3:0]	1	160k/value[3:0], value should not be zero
0x12 ~ 0x13	Charge Pump Current	RW	[11:0]	1	Charge pump current, value * 0.3125uA
0x14	PLL Status	R	[1:0]	0	PLL status indication Bit[0]: LOS, 0: reference is present, 1: reference is lost Bit[1]: Lock, 0: Not locked on reference yet, 1: locked
0x15	MTP Load/Burn Status	RW	[0]	0	Upon power up, IC will load 0x07 ~ 0x13 register value from MTP. This register shows whether the load process is complete, 0: load/burn not complete 1: load/burn complete
0x16	MTP Load status,	R	[0]	0	When MTP load is complete, this register indicates the checksum Checksum 0: Failed 1: Success
0x17	Times of MTP Programmed	R	[7:0]	0	The MTP can be programmed up to 255 times, this value shows how many times the MTP has been programmed
0x18 ~ 0x19	Nearest VCXO to 10kHz Divider Value	RW	[13:0]	0	The nearest integer divider value from VCXO frequency to 10kHz (this provides the internal clock information required for burning the content)

Control Interfaces

The NF1011 is controlled through serial port I2C on pins SCL and SDA.

I2C Format

1. NF1011 default ID is 0x12, or loading from an MTP valid ID.
2. ID is 7-bit, ADR is 8-bit, and DATA is 8-bit.
3. Transmit order is MSB first including ID[6:0], ADR[7:0], DATA[7:0].
4. Both read and write support single byte and multiple bytes access.
5. For multiple bytes mode, the accessed data is starting from the current address ADR[7:0].
6. Abbreviation
   - A: Acknowledge
   - A: No acknowledge
   - S: Start
   - P: Stop
   - R: Read
   - W: Write
   - Sr: Repeated Start

Write Format

Single Byte

S	ID[6:0]	W	A	ADR[7:0]	A	WDATA[7:0]	A	P

Multiple Bytes

S	ID[6:0]	W	A	ADR[7:0]	A	WDATA1[7:0]	A	WDATA2[7:0]	A	P

Read Format 1

Single Byte

S	ID[6:0]	W	A	ADR[7:0]	A	Sr	ID[6:0]	R	A	RDATA[7:0]	$\overline{A}$	P

Multiple Bytes

S	ID[6:0]	W	A	ADR[7:0]	A	Sr	ID{6:0}	R	A	RDATA1[7:0]	A	RDATA2[7:0]	$\overline{A}$	P

Read Format 2

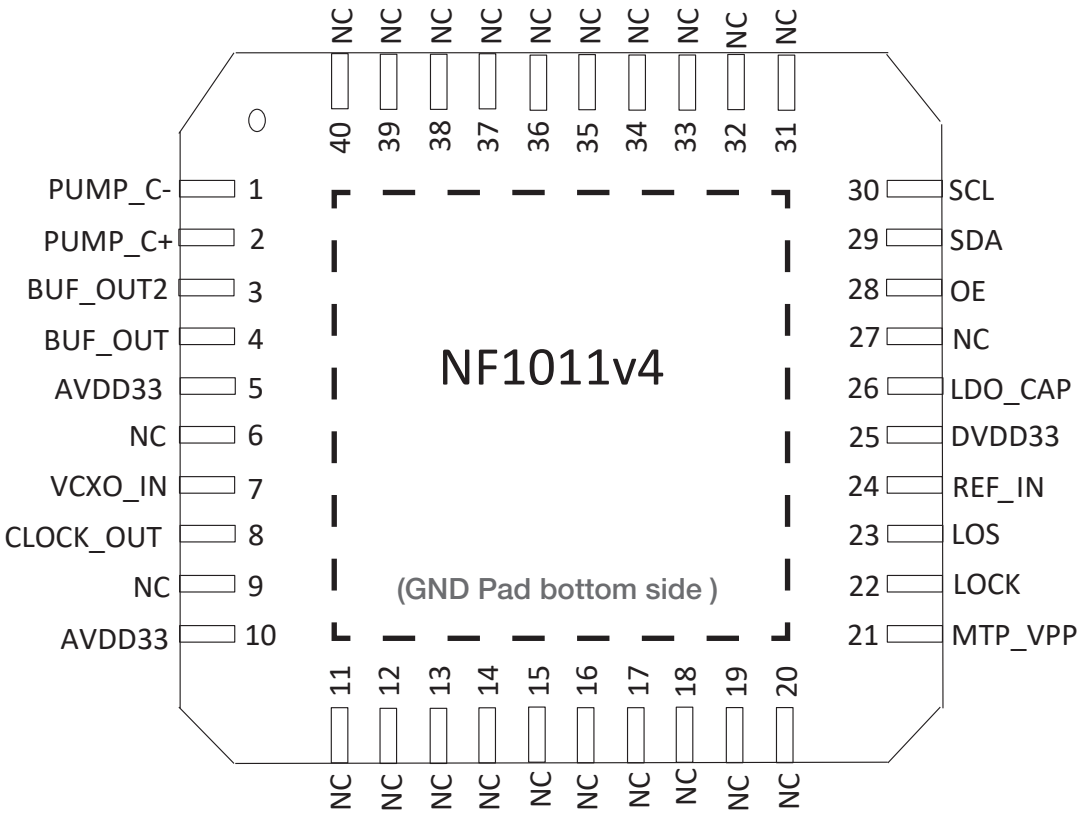
Single Byte

S	ID[6:0]	W	A	ADR[7:0]	A	P
S	ID[6:0]	R	A	RDATA1[7:0]	$\overline{A}$	P

Multiple Bytes

S	ID[6:0]	W	A	ADR[7:0]	A	P
S	ID[6:0]	R	A	RDATA1[7:0]	A	RDATA2[7:0]	$\overline{A}$ P

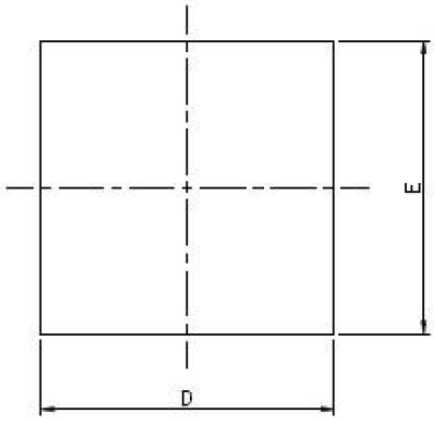
NF1011 Pin Diagram (Top View)



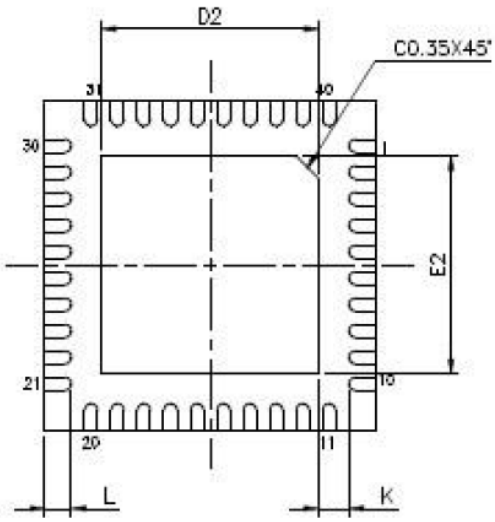
Pin	Description
1	Pump C- Connect to C0 cap negative side
2	Pump C+ Connect to C0 cap positive side
3	BUF_OUT 2 Provide control voltage to VCXO
4	BUF_OUT Provide control voltage to VCXO
5	AVDD33
6	N/C
7	VCXO 3.3V LVCMOS input signal
8	VCXO 3.3V LVCMOS output buffer through IC
9	N/C
10	VDD33_PLL
11-20	N/C
21	MTP_VPP +6.5v power supply pin
22	Lock indication when pin goes HIGH, not locked when pin is LOW
23	Loss of signal (LOS) indiction when pin goes HIGH, reference is present when pin is LOW
24	+3.3V LVCMOS reference input
25	Digital +3.3V power supply
26	LDO Cap (Use 1uF bypass cap to ground for internal LDO)
27	N/C
28	OE Output enable/disable
29	SDA I2C
30	SCL I2C
31-40	N/C
GND Pad	Bottom Ground Pad must be tied to GND.

**All undefined pins should be left floating*

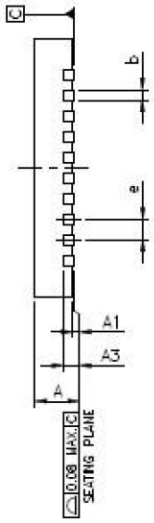
NF1011 Package Dimensions



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		5.00 BASIC	
E		5.00 BASIC	
e		0.40 BASIC	
K	0.20	—	—

PAD SIZE (MIL)	MILLIMETER					
	D2/E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
159X159-G	3.74	3.79	3.84	0.25	0.30	0.35

Revision History

Revision	Date	Note
04	09/28/21	Updates to Registry, Block Diagram and Specifications
05	03/17/22	Update to Specifications and Registry

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