TDC210
DAC based
Compensation IC

General Description

The TDC210 is a highly integrated special purpose ASIC incorporating a a high resolution DAC, internal programmable memory and a powerful processor that enables the disciplining of an external VCOCXO in an open loop circuit.

The TDC210 has a dedicated master I2C port that accepts temp sense data streamed directly from an external temperature sensor. Linear modeling of temperature sensor data and DAC value data can be regressed into multiple segments of up to third order polynomial equations.

Coefficients are stored in internal memory of the TDC210. The TDC210's powerful internal processor reads external temp sense values and actively disciplines the control voltage pin of the VCOCXO. This DAC based open loop system precisely disciplines the oscillator to achieve sub PPB level frequency stability levels over the operating temperature range. First to fourth order delta sigma modulation is available to move spurious modes to higher frequency levels.

Features

- Simple operation dedicated to compensating voltage controlled oscillators
- Hi Resolution DAC with internal processor
- Internal programmable memory bank
- Programmable delta sigma level control
- Stores up to 245 3rd order polynomial segments
- Programmable temp sense update rate
- Master I2C directly reads streaming Temp Sensor data.
- Supports standard I2C bus interface
- Operating temperature range of -40°C to +85°C
- +3.3V operation
- 40-pin QFN package (5mm x 5mm)
- RoHS and REACH compliant

Funcational Block Diagram

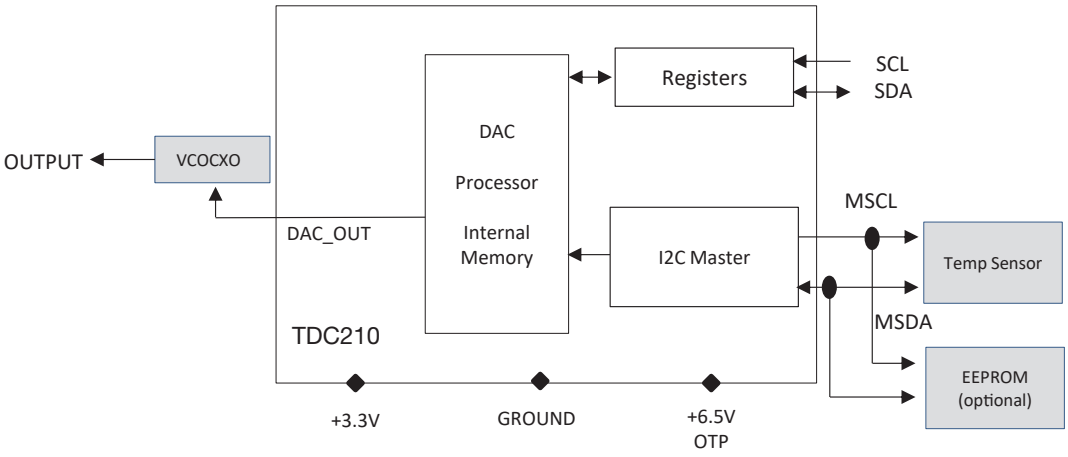


Figure 1 TDC210 Funcational Block Diagram

Bulletin	TM2150
Revision	01
Date	25 Jan 2024

General Description

The TDC210 is designed for the purpose of compensating a high precision voltage controlled OCXO (VCOCXO) to improve stability over temperature error in the VCOCXO. The TDC210 is a highly integrated, special purpose ASIC incorporating a a high resolution DAC, internal programmable memory , a dedicated master I2C port for communicating with an external temperature sensor and an internal processor.

The internal processor accepts temp sensor values from an external temp sensor and calculates a DAC value output from user defined polynomial functions stored in the NC3DC's internal memory structure. This system enables the disciplining of an external VCOCXO in an open loop circuit.

The TDC210,combined with a Texas Instrument TMP116* or AS621x** temp sensor and an VCOCXO can be created to form a compensated oscillator module capable of sub PPB level stability over a defined operating temperature range. Linear modeling of temperature sensor data versus DAC value data generated during a temperature sweep of the module over a defined operating temperature range is required. The IC has a DAC control mode setting that allows the user to control the DAC externally or to be controlled internally by the IC's processor in autonomous mode. In user control mode, data can be collected to generate the linear model and store coefficients for use in autonomous control mode. In autonomous mode, the IC will set the DAC value using temperature sensor values read from the external temp sensor and calculate the DAC value required from the polynomial coefficient information stored.

The TDC210's internal memory has 256 64-byte "page" segments. Each page can store up to a 3rd order polynomial equation's coefficients. Multiple pages can be grouped to form a "table" comprising segments that cover a defined operating temperature range. While the internal OTP is only one time programmable, depending upon the number of segments used to generate a table, multiple tables can be written into the internal OTP memory. Only the last table will be read by the processor. Using an external EEPROM is optional.

The TDC210 can be set up to read temp sensor values at update rates of once per second, twice per second or four times per second. First to fourth order delta sigma modulation is available to move spurious modes to higher frequency levels in the phase noise spectrum.

While the TDC210 can use its internal memory and processor capability to perform the compensation function, an external eeprom and processor can be used in a conventional configuration using I2C ports to enable the DAC functionality.

* https://www.ti.com/product/TMP116

** https://ams.com/documents/20143/36005/AS621x_DS000677_2-00.pdf

One Time Programming (OTP) Memory

The OTP can contain multiple coefficient tables, but only the one in highest address is used.

Each table contains multiple segments of 3rd order polynomial coefficient and the associate temperature range. The number of byte for the table is number of segment * 34 + 14. In OTP, each page has 64 byte and the programmable unit is page. As such, the next table must start from next page of last page of current table.

In each table, the 1st byte is 0xaa to indicate the table is valid.

The 2nd byte stores the number of segments being used.

The 3rd byte stores the temp sensor type being used.

The 4th byte stores the update rate value of the temp sensor. The temp sensor update rate can be 1 time per second, 2 times per second or 4 times per second.

The 5th bye stores the order of delta sigma chosen. The delta Sigma order level can be chosen from first order to fourth order.

The temp boundary value starts from the 15th byte. If there are "n" segments, a boundary value of (n – 1) is required. Each value is 2 bytes. The boundary value order is from low to high. Each segment has 4 8-byte (LSB) floating point coefficients. The first coefficient is for order 0, second coefficient is for order 1, third coefficient is for order 2, and the fourth coefficient is for order 3.

Assuming the segment is from S0, S1, to Sn, and temp boundary value is from T1, T2, to Tn. If the temp value is < T1, segment S0 coefficient will be used. If the temp value is >= Tn, segment Sn coefficient will be used. If temp value is >= Tx and < T(x+1), the segment Sx coefficient will be used.

There are 256 "pages" available in the OTP. Each page has 64 bytes. The OTP can only be programmed in page mode.

To program a page into OTP:

Step 1: Apply 6.5V to MTP_VPP pin 21

Step 2: Check to see that OTP read/write is in ready mode. This is done by reading reg 0xa4. If bit[1] is 0, it is in ready mode, otherwise it is not in ready mode.

Step 3: Set the page number in reg 0xa1.

Step 4: Write 64 byte contents to reg 0xc0 ~ 0xff.

Step 5: Write 0 to reg 0xa4

Step 6: When reg 0xa4 bit[1] is 0, the program is done.

To read a page from OTP to reg 0xc0 ~ 0xff:

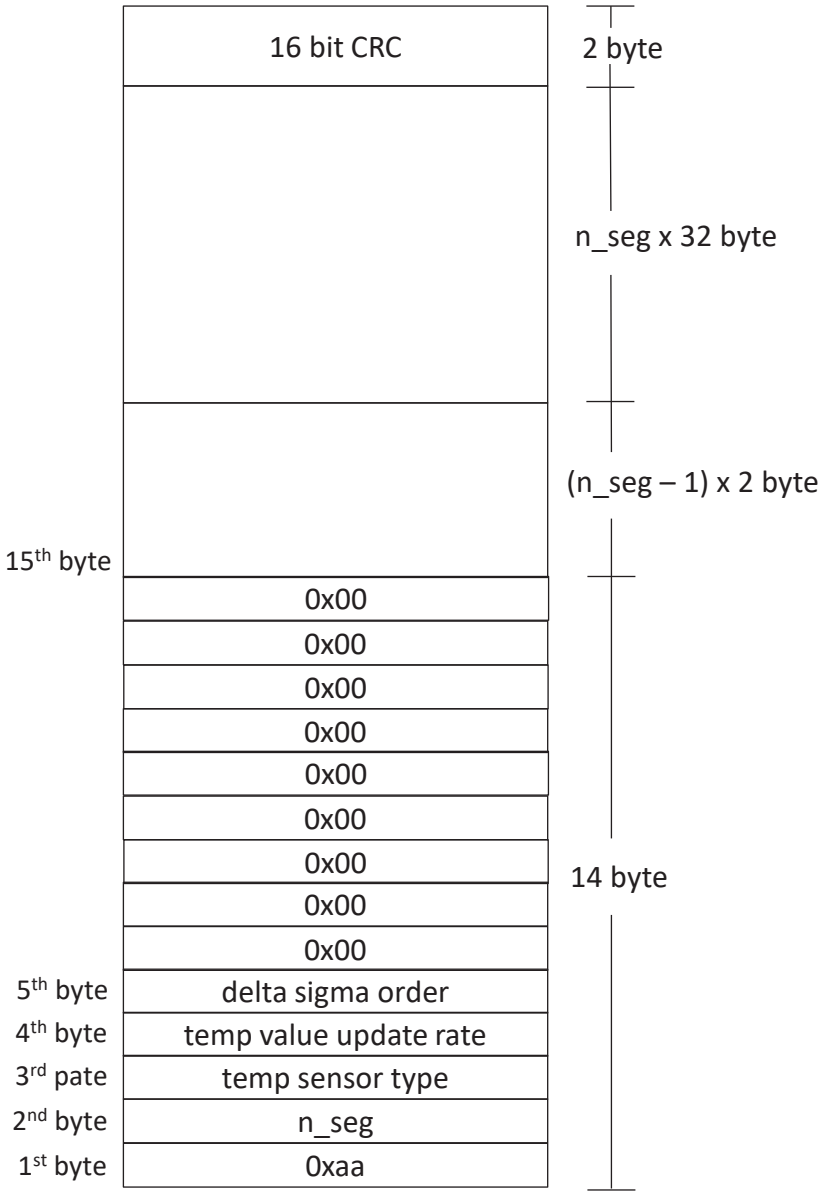
Step 1: Check to see that OTP read/write is in ready mode by reading reg 0xa4. If bit[1] is 0, then it is in ready mode, otherwise it is not ready.

Step 2: Set the page number in reg 0xa1.

Step 3: Write 1 to reg 0xa4.

Step 4: When reg 0xa4 bit[1] is 0, the read is complete

Coefficient Table



TDC210 Register Table

I/O = R Read only
I/O = W Write only
I/O = r/W Write, but previous written value could be read-back
I/O = R/W Read and Write

ADDR	BITS	NAME	I/O	DESCRIPTION
0x00~0x05	6 x [7:0]	Chip_ID	R	Chip ID, from byte #0 to byte #5
0x06	[7:0]	Chip_REV	R	Chip Revision
0x07	[13:0]	WORKSHEET_ADDR	R	The MTP address base of the found worksheet
0x09	[7:0]	SEGMENT_NUM	R	The temperature segment number specified in the founded worksheet
0x0A	[0]	TEMP_SENSOR_TYPE	r/W	To specify the temperature sensor type
0x0B	[1:0]	TEMP_READING_RATE	r/W	To specify the reading rate of the temperature sensor
0x0C	[1:0]	DITHER_ORDER	r/W	To specify the dithering order of this Delta-Sigma DAC
0x0D~0x15				~RSVD~
0x16	[15:0]	TEMP_VALUE	R	The last value of the temperature sensor reading
0x18	[0]	CONTROL_MODE	r/W	To specify the DAC control mode
0x19~0x1C	[27:0]	DAC_VALUE_AUTO	R	The DAC value determined, in automatic control mode
		DAC_VALUE_MANUAL	r/W	To specify the DAC value, in manual control mode
0x1D~0x9F				~RSVD~
0xA0	[2:0]	LOAD_STS	R	MTP Load Status
0xA1	[7:0]	MTP_PAGE_INDEX	r/W	To specify the page index of MTP read/write operations
0xA2~0xA3				~RSVD~
0xA4	[0]	MTP_CMD	W	MTP read/write operation command
	[1:0]	MTP_STS	R	MTP read/write operation status
0xA5	[11:0]	MTP_PWE_TIMER	r/W	To specify MTP programming timer value
0xA7	[0]	PERIPHERAL_I2C_BUS_STS	R	The status of the peripheral I2C bus
0xA8~0xBF				~RSVD~
0xC0~0xFF	64 x [7:0]	MTP_PAGE_BUFFER, Byte 0~63	R/W	The 64-byte page buffer for MTP read/write operations

TDC210 Registereed Detail Description

ADDR	BITS	NAME	I/O	VALUE	DESCRIPTION
0x00	[7:0]	Chip_ID Byte 0	R	'T'	Chip ID, ASCII String "TCD210"
0x01	[7:0]	Chip_ID Byte 1	R	'C'	
0x02	[7:0]	Chip_ID Byte 2	R	'D'	
0x03	[7:0]	Chip_ID Byte 3	R	'2'	
0x04	[7:0]	Chip_ID Byte 4	R	'1'	
0x05	[7:0]	Chip_ID Byte 5	R	'0'	
0x06	[7:0]	Chip_REV	R	1	Chip Revision
0x07	[13:0]	WORKSHEET_ADDR	R		The MTP address base of the found worksheet
0x09	[7:0]	SEGMENT_NUM	R		The temperature segment number of the founded worksheet
0x0A	[0]	TEMP_SENSOR_TYPE	r/W	0	To specify the temperature sensor type 0: TI TMP116/117 or compatible 1: AMS AS621X or compatible
0x0B	[1:0]	TEMP_READING_RATE	r/W	0	To specify the reading rate set to the temperature sensor 0: STOP, no update at all 1: 1 time/sec 2: 2 times/sec 3: 4 times/sec <ps> Must set to 0 when programming MTP
0x0C	[1:0]	DITHER_ORDER	r/W	0	To specify the dithering order of this Delta-Sigma DAC 0: 1st order 1: 2nd order 2: 3rd order 3: 4th order
0x0D~0x15					~RSVD~
0x16	[15:0]	TEMP_VALUE	R		The last value of the temperature temperature sensor reading
0x18	[0]	CONTROL_MODE	r/W	0	To specify the DAC control mode 0: automatic control mode 1: manual mode (manipulated by users)
0x19	[27:0]	DAC_VALUE_AUTO	R		The DAC value determined by IC, in automatic control mode
		DAC_VALUE_MANUAL	r/W	0x7FF.FFFF	To specify the DAC value, in manual control mode
0x1D~0x9F					~RSVD~

ADDR	BITS	NAME	I/O	VALUE	DESCRIPTION
0xA0	[2:0]	LOAD_STS	R		MTP Load Status bit[0] load condition 0: not complete yet 1: completed bit[1] MTP content 0: not valud 1: valid bit[2] MTP content checksum status 0: FAIL 1: SUCC
0xA1	[7:0]	MTP_PAGE_INDEX	r/W	0	To specify the page index of MTP read/write operations
0xA2~0xA3					~RSVD~
0xA4	[0]	MTP_CMD	W		MTP read/write operation command (0) to initiate writing a 64-byte page content from the MTP PAGE BUFFER to a page on the MTP memory (1) to initiate the reading of a 64-byte pagae content from MTP memory to the MTP PAGE BUFFER
	[1:0]	MTP_STS	R		MTP read/write operation status bit[0] operation 0: write operation, 1: read operation bit[1] operation status 0: ready/done, 1: not ready
0xA5	[11:0]	MTP_PWE_TIMER	r/W	2333	To specify MTP programming timer value <ps> This value must be set to 2500 before doing MTP programming
0xA7	[0]	PERIPHERAL_I2C_BUS_STS	R		~The status of the peripheral I2C bus 0: IDLE/READY 1: BUSY
0xA8~0xBF					~RSVD~
0xC0	[7:0]	MTP_PAGE_BUFFER, Byte 0	R/W		
0xC1~0xFE	[7:0]	MTP_PAGE_BUFFER, Byte 1..62	R/W		The 64-byte page buffer for MTP read/write operations
0xFF	[7:0]	MTP_PAGE_BUFFER, Byte 63	R/W		

Control Interfaces

The TDC210 is controlled through serial port I2C on pins SCL and SDA.

I2C Format

1. TDC210 default ID is 0x12, or loading from an OTP valid ID.
2. ID is 7-bit, ADR is 8-bit, and DATA is 8-bit.
3. Transmit order is MSB first including ID[6:0], ADR[7:0], DATA[7:0].
4. Both read and write support single byte and multiple bytes access.
5. For multiple bytes mode, the accessed data is starting from the current address ADR[7:0].
6. Abbreviation
   - $\overline{A}$: Acknowledge
   - A: No acknowledge
   - S: Start
   - P: Stop
   - R: Read
   - W: Write
   - Sr: Repeated Start

Write Format

Single Byte																
S	ID[6:0]	W	A	ADR[7:0]	A	WDATA[7:0]									A	P
Multiple Bytes																
S	ID[6:0]	W	A	ADR[7:0]	A	WDATA1[7:0]			A	WDATA2[7:0]					A	P

Read Format 1

Single Byte																
S	ID[6:0]	W	A	ADR[7:0]	A	Sr	ID[6:0]	R	A	RDATA[7:0]					$\overline{A}$	P
Multiple Bytes																
S	ID[6:0]	W	A	ADR[7:0]	A	Sr	ID{6:0}	R	A	RDATA1[7:0]	A	RDATA2[7:0]			$\overline{A}$	P

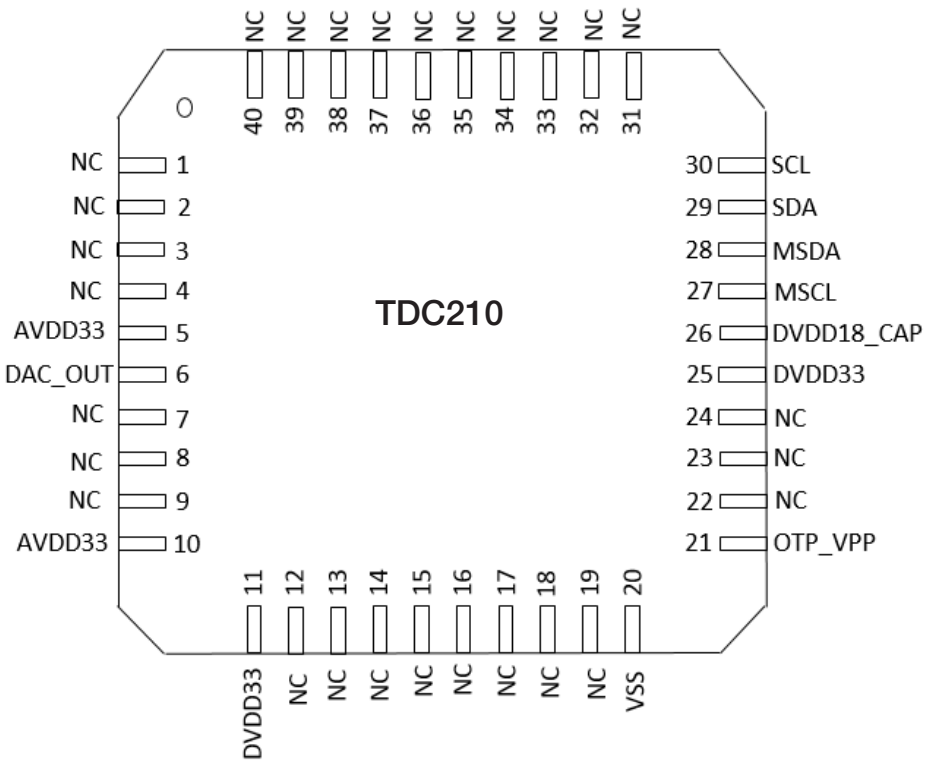
Read Format 2

Single Byte																
S	ID[6:0]	W	A	ADR[7:0]											A	P
S	ID[6:0]	R	A	RDATA1[7:0]											$\overline{A}$	P
Multiple Bytes																
S	ID[6:0]	W	A	ADR[7:0]											A	P
S	ID[6:0]	R	A	RDATA1[7:0]	A	RDATA2[7:0]									$\overline{A}$	P

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the lead frame chip scale package (CP-40L) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the lead frame chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided. Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated into the thermal pad at a 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm and the via barrel should be plated with 1 oz copper to plug the via. The user should connect the printed circuit board thermal pad to AGND.

Figure 4: TDC210 5x5mm QFN Pin Diagram (Top View)

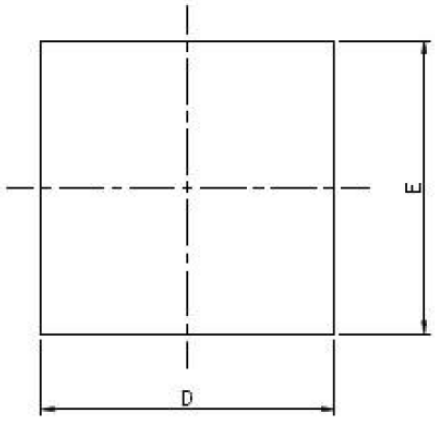


Pin Descriptions

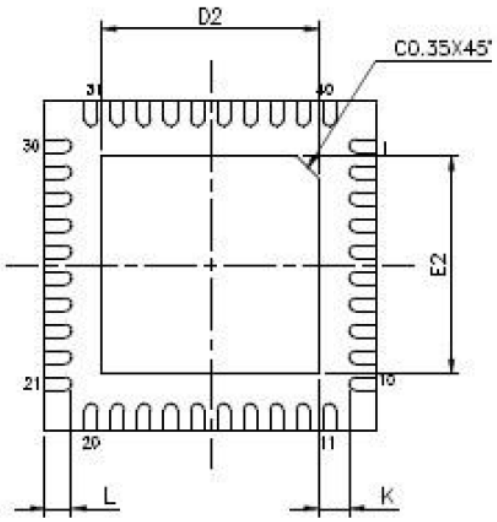
Pin	Description
1-4	NC
5	Analog +3.3v power supply
6	DAC_OUT
7-9	NC
10	Analog +3.3v power supply
11	Digital +3.3v power supply
12-19	NC
20	VSS
21	OTP_VPP +6.5v power supply pin
22-24	NC
25	Digital +3.3v power supply
26	LDO Cap Internal digital 1.8v, should connect 1uF bypass cap
27	MSCL
28	MSDA
29	SDA I2C
30	SCL I2C
31-40	N/C

**All undefined pins should be left floating*

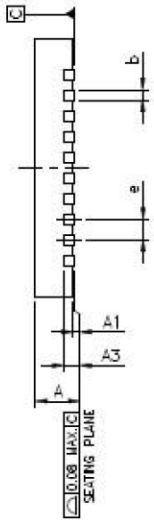
TDC210 Package Dimensions



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		5.00 BASIC	
E		5.00 BASIC	
e		0.40 BASIC	
K	0.20	—	—

PAD SIZE (MIL)	MILLIMETER					
	D2/E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
153X153-G	3.25	3.30	3.35	0.35	0.40	0.45
159X159-G	3.74	3.79	3.84	0.25	0.30	0.35

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Revision History

Revision	Date	Note
00	12/13/23	TDC210 release
01	01/25/04	Updated block diagram and product inforrmation