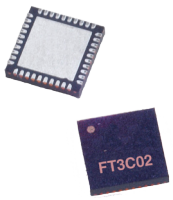
DATA SHEET

FT3C02
Auto-Compensating Frequency Translator ASIC

Overview

The FT3C02 is a highly integrated clock frequency translation IC designed to receive a 10MHz clock input signal and generate up to two frequency-translated single-ended clock outputs, phase locked to the incoming 10MHz source. The FT3C02 supports virtually any 10.00 MHz 3.3V clock signal as the input to the module for translating to the output frequency. However, the primary feature of the FT3C02 is its auto-calibration function used to compensate specially designed OCXO modules. Using a Connor Winfield Temperature Sense Enabled (TSE) OCXO, the FT3C02 will automatically calibrate and apply frequency offset adjustments to compensate for OCXO's normal frequency instability due to thermal changes over its stated operating temperature range. A TSE OCXO module such as OH20TSE-10M can be compensated to ±0.2ppb over the specified operating temperature range.



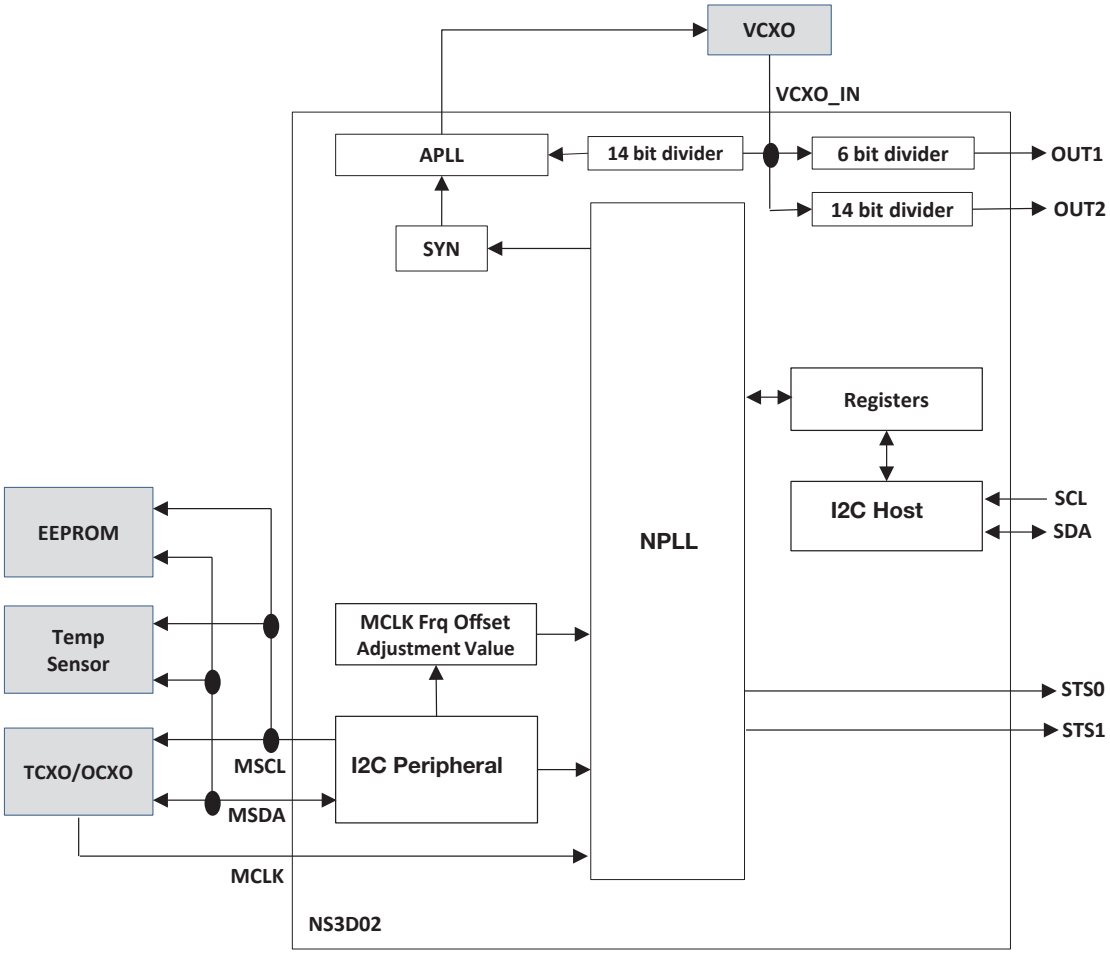
A user supplied external VCXO disciplined by the FT3C02's analog PLL system provides the output characteristics for phase noise and jitter performance for the two single ended clock outputs available to the user. The FT3C02 supports low jitter performance at frequencies up to 156.25MHz, which can also be further divided down at the output ports with 6- and 14-bit divider values.

This product can be used to support a high-stability frequency reference for use in wireless systems, IEEE 1588v2, and any application that requires frequency translation.

Features

- 10 MHz MCLK input
- Generates one or two 3.3V single ended Low Jitter Clock Outputs derived from external VCXO
- Supports up to 156.25MHz external VCXO clock output frequency range
- Programmable output dividers from external VCXO frequency
- Automatic compensation when using external TSE (Temp Sense Enabled) OCXO modules.
- I2C Interface for system communication and programming.
- 3.3VDC Supply Voltage
- -40°C to 105°C operating temperature range
- 5 x 5mm 40 pin QFN surface mount package

FT3C02 Functional Block Diagram



Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	125	°C	
Supply Voltage	-0.5	-	4.5	Vdc	
Operating Supply Voltage 3.3 Vdc	3.13	3.30	3.47	Vdc	

Absolute Ratings: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only. The functional operation of the device at those or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to conditions outside the "recommended operating conditions" for any extended period of time may adversely impact device reliability and result in failures not covered by warranty.

Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Supply Voltage (AVDD33, DVDD33)	3.13	3.30	3.47	Vdc	
Supply Current		100		mA	
Oeprating temperature Range	-40	-	105	°C	

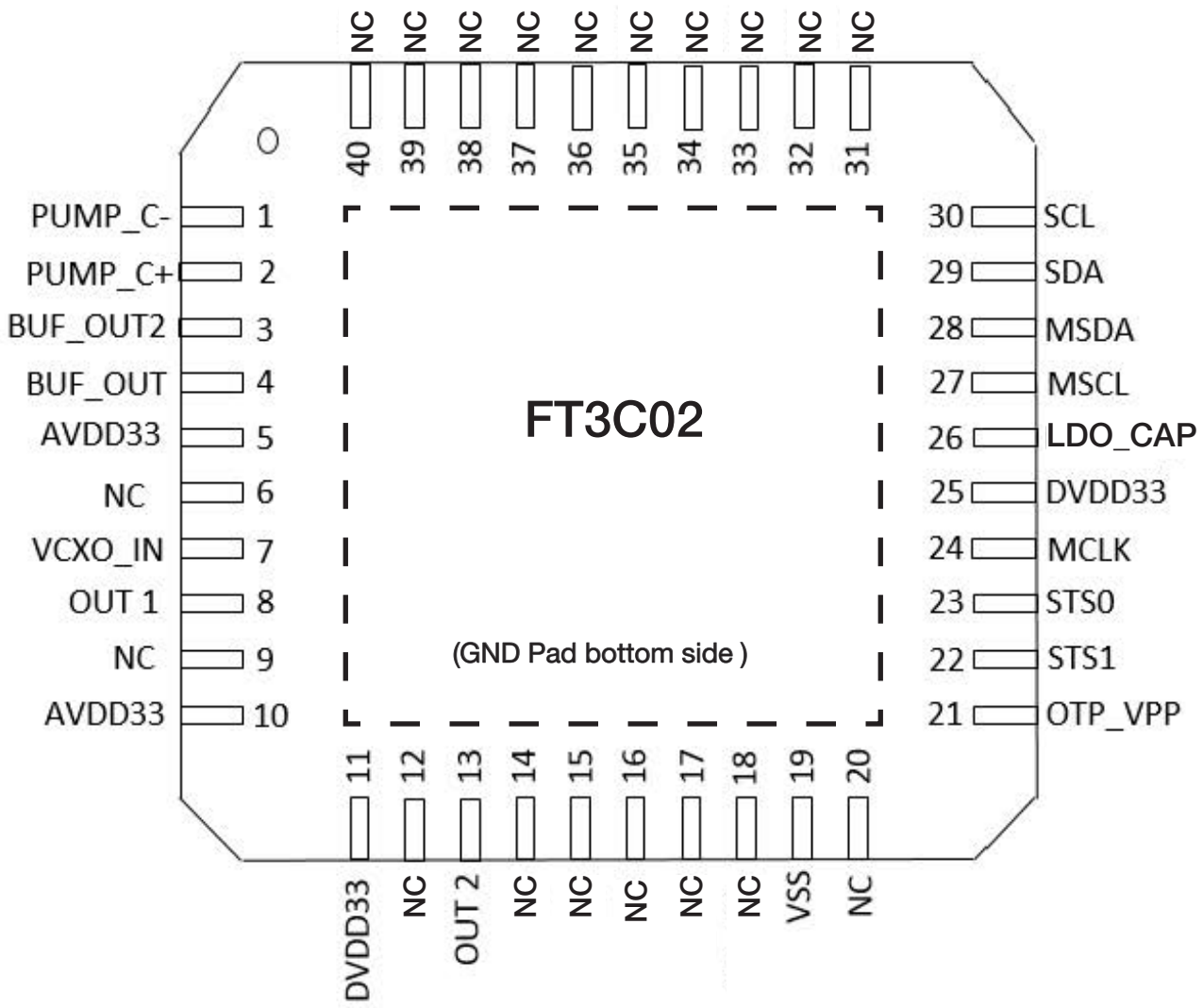
LVCMOS Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	15	-	pF	
Output Voltage					
(High) (Voh)	3.0	-	-	V	
(Low) (Vol)	-	-	0.4		
Duty Cycle at 50% of Vcc	45	50	55	%	
Rise / Fall Time 10% to 90%	-	-	6	ns	

Package Characteristics

Package	5 x 5 x 1mm 40 pin QFN Package
Moisture Sensitivity Level	MSL-3

FT3C02 Pin Assignments (Top View)



Pin Connection Recommendations

- VDD Pins and Decoupling: all VDD pins must always be connected.
- Unused Clock Outputs: leave unused clock outputs floating and powered down.
- All NC (no connection) pins should be left floating.

FT3C02 Pin Description

Pin No.	Pin Name	I/O	Description
1	PUMP_C-		Connect to APLL's external filter -
2	PUMP_C+		Connect to APLL's external filter +
3	BUFF_OUT2		Connect to VCXO voltage control pin (connecting to filter cap)
4	BUFF_OUT		Connect to VCXO voltage control pin (connecting to filter cap)
5	AVDD33	Power	3.3V Analog power input
6	NC		
7	VCXO_IN	I	Accepts VCXO's 3.3V LVCMOS clock output
8	OUT_1	O	3.3V LVCMOS Output
9	NC		
10	AVDD33	Power	3.3V Analog power input
11	DVDD33	Power	3.3V Digital power input
12	NC		
13	OUT_2	O	3.3V LVCMOS Output
14	NC		
15	NC		
16	NC		
17	NC		
18	N/C		
19	VSS	Power	GROUND
20	NC		
21	OTP_VPP	Power	6.5V power input while programming OTP
22	STS1	O	Status Pin
23	STS0	O	Status Pin
24	MCLK	I	Master Clock input. Accepts 3.3V LVCMOS clock signal input
25	DVDD33	Power	3.3V Digital Power input
26	LDO_CAP		Connect internal LDO to external MLCC Capacitor to GND (~1 uF)
27	MSCL	I	Master Serial Clock Output. Communicates with data from Temp Sensor
28	MSDA	I	Master Serial Data. Accepts data from Temp Sensor
29	SDA	I/O	Serial Data
30	SCL	O	Serical Clock Output
31	NC		
32	NC		
33	NC		
34	NC		
35	NC		
36	NC		
37	NC		
38	NC		
39	NC		
40	NC		

General Description

The FT3C02 design architecture incorporates a sophisticated digital and analog PLL scheme to provide 2 low jitter phase/frequency locked clock outputs at frequencies from 8 kHz to 160 MHz The system is clocked with an external 10MHz OCXO or TCXO providing the basis for various performance options.

The chip digitally synthesizes one output from its timing generator, which is sent to an analog PLL stage. The analog portion of the chip consists of an independent APLL circuit with integrated charge pump and phase detector, supported by an external VCXO, that translates the frequency and attenuates the jitter on the synthesized clock output generated in the NPLL section of the chip. Two single ended output clocks are derived from the disciplined VCXO. The external VCXO chosen provides the output characteristics for phase noise and jitter performance for the 2 clock outputs generated by the IC. The two LVCMOS level clock output transmitters have follow on divider circuits available. Output 1 has a 6-bit divider capability, while output 2 has a 14-bit divider capability.

The FT3C02 has functionality for manually or automatically creating frequency offsets in its internal numerically controlled oscillator (NCO) which is supported by an external master clock. A register is available for making manual offsets and via register settings, the automatic compensation scheme can be enabled. A peripheral I2C bus connection supports direct communication with OCXO modules enabled with compatible temperature sense enabled (TSE) circuitry.

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Internal NPLL and Numeric Timing Generator

The kernel of the FT3C02 is a NPLL (Numerical-based PLL). In its core, all internal modules are either digital or numerical, including the phase detectors, filters, timing generator and clock synthesizers. The pure digital design timing generator allows the FT3C02 to become an accurate and reliable deterministic system.

An internal clock synthesizer generates an internal clock signal at any frequency from 40kHz to 1MHz in 8kHz step to act as the reference input to the follow-on APLL (Analog PLL). The APLL's clock is fanned out to two clock output ports, each has its own post divider to divide down the frequency.

The FT3C02's timing generator is clocked by a fixed frequency external LVCMOS-level 10MHz clock source as its master clock (MCLK).) The MCLK input characteristics could be provided by virtually any 10.0MHz source but an OCXO or a high precision TCXO are recommended.

FT3C02 Register Table

I/O Description: R = Read Only; W = Write Only; r/W = Write, but previous written value could be read back; R/W = Read and Write

ADDR	BITS	REGISTER NAME	I/O	DESCRIPTION
0x00~0x06	7 x [7:0]	Chip_ID	R	Chip ID, from byte #0 to byte #6
0x07	[7:0]	Chip_REV	R	Chip Revision of FT3C02
0x08	[7:0]	FW_REV	R	Firmware Revision of FT3C02
0x09~0x0F				~RSVD~
0x10	[7:0]	APLL_REF_FREQ	r/W	The frequency of APLL's input reference synthesizer
0x11	[13:0]	APLL_FB_DIV	r/W	APLL's feedback divider
0x13	[0]	APLL_R0_CHOICE	r/W	APLL's R0 choice
0x14	[8:0]	APLL_R0_VALUE_L	r/W	APLL's R0_VALUE_L resistance selection
0x16	[4:0]	APLL_R0_VALUE_S	r/W	APLL's R0_VALUE_S resistance selection
0x17	[3:0]	APLL_R2_DIV	r/W	APLL's R2 resistance
0x18	[11:0]	APLL_CP_CURRENCY	r/W	APLL's charge pump currency
0x1A	[7:0]	TEST_MODE1	r/W	TEST MODE1 (for internal use only). MUST BE 0
0x1B	[7:0]	TEST_MODE2	r/W	TEST MODE2 (for internal use only). MUST BE 0
0x1C	[7:0]	TEST_MODE3	r/W	TEST MODE3 (for internal use only). MUST BE 4
0x1D~0x1F				~RSVD~
0x20	[1:0]	MCLK_TEMPCO_SRC	r/W	MCLK Temperature Compensation Coefficient Source Selection
0x21	[0]	MCLK_TEMP_SENSOR_TYPE	r/W	Temperature Sensor Type for MCLK Temperature Compensation
0x22	[0]	MCLK_AUTO_TEMP_ADJ_REVERSE	r/W	To reverse MCLK Temperature Compensation Polarity
0x23~0x3F				~RSVD~
0x40	[5:0]	OUT1_POST_DIV	r/W	OUT1 Post Divider
0x41	[13:0]	OUT2_POST_DIV	r/W	OUT2 Post Divider
0x43	[31:0]	MCLK_USER_ADJ	r/W	User specified MCLK adjustment
0x47	[0]	MCLK_USE_AUTO_TEMP_ADJ	r/W	Selection of using automatic MCLK temperature compensation calculation
0x48	[1:0]	MCLK_TEMP_SENSOR_RATE	r/W	Temperature Sensor Reading Rate
0x49~0x4F				~NOT USED~
0x50	[15:0]	MCLK_TEMP_SENSOR_VALUE	R	MCLK Temperature Sensor Raw Reading
0x52	[31:0]	MCLK_AUTO_TEMP_ADJ_RESULT	R	MCLK Temperature Compensation Calculation Result
0x56	[31:0]	MCLK_TOTAL_ADJ	R	MCLK total adjustment
0x5A~0x7F				~NOT USED~
0x80	[7:0]	MCLK_TEMPCO_PAGE_IDX	R	EEPROM Page Index of found MCLK Temperature Coefficients
0x81~0x9F				~RSVD~
0xA0	[5:0]	LOAD_STATUS	R	OTP/EEPROM loading status
0xA1	[7:0]	EEP/OTP_PAGE_IDX	r/W	Target EEPROM/OTP read/write page index
0xA2	[0]	EEPROM_CMD	W	EEPROM command
	[2:0]	EEPROM_STS	R	EEPROM status
0xA3	[7:0]	SOFT_RESET	W	IC Soft Reset Command
0xA4	[0]	OTP_CMD	W	OTP command
	[1:0]	OTP_STS	R	OTP status
0xA5	[11:0]	OTP_PWE_TIMER	r/W	OTP PWE Timer
0xA7	[0]	Peripheral_I2C_BUS_STS	R	Peripheral I2C bus Master Controller status
0xA8~0xBF				~RSVD~
0xC0~0xFF	64 x [7:0]	PAGE_BUFFER	R/W	EEPROM/OTP read/write page buffer, from byte#0 to byte#63

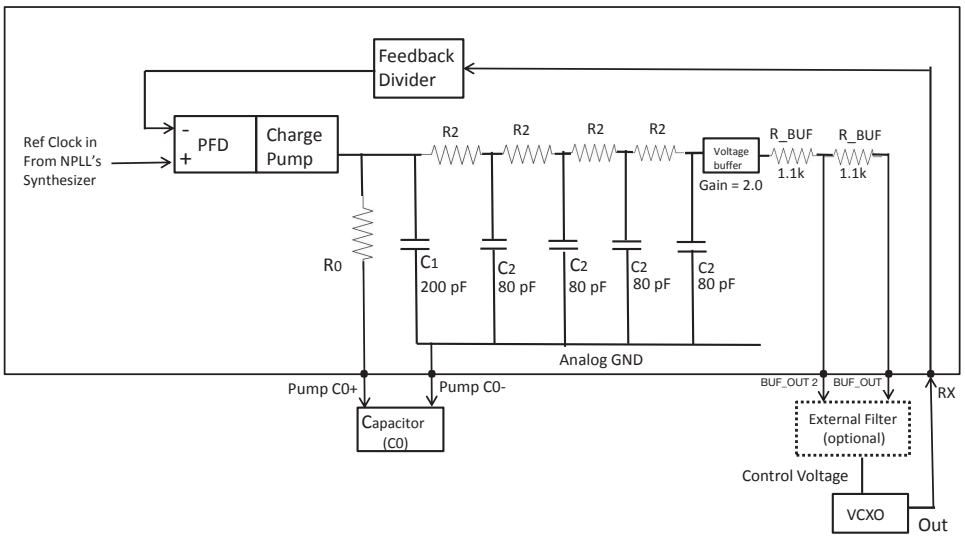
Detailed Description

APLL Configuration

The analog PLL (APLL)'s function in FT3C02 is to discipline the external VCXO to output up to two divided down clocks. The APLL will take a clock synthesized by the NPLL as its reference input, translate the frequency to higher frequency and also attenuate the jitter generated by NPLL's digital clock synthesizer.

FT3C02's APLL circuit contains a phase frequency detector (PFD), a programmable charge pump, an uncompleted programmable passive low-pass filter (LPF), a fixed-gain voltage buffer, and a programmable clock feedback divider. With some extra external capacitors to complete the LPF, the APLL can operate to cover loop bandwidth ranging from 10Hz to 200 Hz easily.

APLL Circuit Diagram



The APLL's input reference is synthesized from the NPLL and can be programmed to have frequency from 40kHz to 1MHz, in 8kHz step, by configuring the register APLL_REF_FREQ. The charging pump could be programmed to have current ranging from 0.3125uA to 1,280uA by configuring the register APLL_CP_CURRENT. Users must add an external capacitor C0 (connecting to pin PUMP_C0+ and pin PUMP_CO-) to complete the passive LPF. This passive LPF includes a programmable resistor R0, an external capacitor C0, a fixed capacitor C1, 4 programmable resistors R2 (R21~4), and 4 fixed capacitors C2 (C21~4). Those programmable resistors could be configured by register APLL_R0_CHOICE, APLL_R0_VALUE_L, APLL_R0_VALUE_S and APLL_R2_DIV.

The voltage buffer has a fixed-gain of x2. The buffer also provides the impedance isolation between the internal LPF and the VCXO's voltage control pin. The output of the buffer goes through two internal serial resistors, each has 1.1k ohm resistance. The end of these two resistors connects to pin BUF_OUT, and the center-tap of these two resistors connects to pin BUF_OUT2. Users could simply connect from either one to VCXO's control voltage pin directly or build a more sophisticated post filter utilizing these two existing internal resistors by adding some external capacitors. The last part of the APLL circuit is the internal programmable non-fractional feedback divider, configured by the 14-bit register APLL_FB_DIV.

Clock/Pulse Outputs

The FT3C02 generates up to two 3.3V LVCMOS level clock outputs on two output transmitter ports.

Output transmitter ports OUT1 and OUT2 are driven by clocks divided down from APLL's external VCXO clock. The output ports consist of a single ended 3.3Vdc CMOS level transmitter. Output transmitters can be disabled if not in use. The LVCMOS output transmitter driving capability is 12 mA.

In front of each output port, a programmable divider is available to divide down the clock from VCXO. The divider at OUT1 is a 6-bit divider, capable of dividing from 1 to 63 or shut-off. OUT2 has a 14-bit divider, capable of dividing from 2 to 16,383 or shut-off. Please pay attention that OUT2 doesn't support to output the same frequency of the VCXO. These two dividers could be programmed by register OUT1_RT_POST_DIV and OUT2_RT_POST_DIV. Both of them are adjustable in run-time.

MCLK Frequency Offset Compensation

The FT3C02 takes its MCLK clock from an external fixed frequency 10MHz MCLK oscillator input on the MCLK_IN pin. However, free running clock oscillators generally have a calibration error as well as a temperature-caused frequency offset away from its nominal frequency. FT3C02 provides users an ability to make adjustments to compensate the frequency offset. While receiving the external MCLK clock, FT3C02 could apply an additional frequency offset adjustment to the it while converting into the internal MCLK system clock by simply programming register MCLK_RT_USER_CALI. As a run-time control register, this feature is suitable to not only compensate its original calibration error but also the run-time frequency offset, such as thermal-caused frequency offset, during system operation.

In addition, the FT3C02 is capable of automatically calculating the thermal frequency offset of the external MCLK oscillator by itself using a stateless polynomial function to convert from the ambient temperature to projected frequency offset. With an external temperature sensor and a set of temperature coefficients of the polynomial function for the oscillator thermal stability characteristics, the FT3C02 can calculate the external oscillator's projected frequency offset and apply a compensating offset adjustment to its own MCLK calibration automatically without the need of an external micro-controller.

MCLK Automatic Frequency Offset Projection

The FT3C02 uses a stateless 5th order polynomial function to project its external MCLK oscillator's frequency offset. The coefficients of this polynomial function could either be extracted from some certain OCXO directly (e.g., Connor-Winfield OH320-CC), or be stored in an external EEPROM or in the FT3C02's internal MTP/OTP non-volatile memory. The FT3C02 was designed to automatically probe certain models of temperature sensors to gather the temperature reading by itself and then calculate the projected frequency offset by applying each temperature reading to the polynomial function. The coefficient source and the temperature sensor type could be configured in register MCLK_TEMPCO_SRC and register MCLK_TEMP_SENSOR_TYPE. The temperature reading and the calculated projected frequency offset could be read back from register MCLK_TEMP_SENSOR_VALUE and register MCLK_AUTO_ADJ_RESULT. Users could set FT3C02's temperature reading rate by programming register MCLK_RT_TEMP_SENSOR_RATE, to either holding the reading, or be 1, 2, or 4 times/sec. FT3C02 support two different temperature sensor model, either Texas Instruments' TMP116/117 or AMS's AS621X. The temperature coefficients could be stored on the same EEPROM used for field upgrade. The EEPROM has to be ATMEL's AT24C128C, or other compatible parts. Both the temperature sensor and the EEPROM have to be located on the Peripheral I2C bus. Users don't need to program the temperature sensor. FT3C02 will initialize the temperature sensor by itself. The I2C addresses of the temperature sensor and the EEPROM will be defined in later I2C bus document section. Be aware that the temperature reading rate could be programmed in run-time. The format used to store the temperature coefficients on the internal MTP/OTP and the external EEPROM will be illustrated later on another sector.

MCLK Compensation, Manual plus Automatic

The FT3C02 could take the MCLK calibration values from both register MCLK_RT_USER_CALI combined with the automatic projected frequency offset calculation result. Register MCLK_USE_AUTO_TEMP_ADJ could be configured to define whether the MCLK calibration taken on only the manual value from register MCLK_RT_USER_CAL, or both the manual value plus the run-time calculation result. Manufacturer's temperature coefficients could be either for projecting its thermal frequency offset or the needed adjustment to compensate this offset. Register MCLK_TEMP_ADJ_REVERSE could be configured to define the polarity of how the calculation result combines to the manual user calibration values. Be aware of that both MCLK_USE_AUTO_TEMP_ADJ and MCLK_TEMP_ADJ_REVERSE are configuration registers. This means that they could not be changed in run-time. The boolean of register MCLK_USE_AUTO_TEMP_ADJ will not affect the temperature reading and the calculation result. This also means that even if MCLK_USE_AUTO_TEMP_ADJ was set to FALSE, users could still utilize FT3C02's automatic temperature reading and frequency offset projection calculation

The Conflict between MCLK Automatic Temperature Reading and Other Operations

The operation of the automatic temperature sensor reading could not coexist with some other operations, including any other peripheral I2C bus activity, operating by this FT3C02 or others, and the MTP/OTP memory read and write. The automatic temperature reading has to be put into hold by programming register MCLK_RT_TEMP_SENSOR_RATE in advance of these operations. For example, the reading needs to be turned off before accessing (reading/writing) to either the external EEPROM or the internal MTP/OTP.

For safety, it is recommended to make the peripheral I2C bus a module's private local I2C bus containing only the temperature sensor and the EEPROM, or the compatible OCXO such like Connor-Winfield's OH20TSE.

I2C Buses

FT3C02 has two I2C controllers, one master controller for its peripheral I2C interface and one slave controller for its host I2C interface. Both I2C interfaces are compliant to the multi-device I2C bus standard. A user's host controller could manipulate the FT3C02 by accessing the internal registers using the host I2C interface via pin SDA and SCL.

The FT3C02 provides access to some certain external peripheral parts like MCLK oscillator modules that have the requisite internal circuitry to help projecting its frequency offset for auto calibration, external EEPROMs, and temperature sensor components using the peripheral I2C interface via pin MSDA and MSCL.

All the peripheral parts OCXO-CC, temperature sensor, and the external EEPROM for automatic MCLK frequency offset compensation, field upgrade, and parameter initialization shall be placed on the Peripheral I2C bus interfacing via pin MSDA and MSCL. To access FT3C02, user's host controller shall use the Host I2C bus interfacing via pin SDA and SCL.

For I2C bus, parts on the same bus cannot share I2C ID addresses. The FT3C02 could be configured up to 4 different ID addresses to support multiple IC's existence on the same I2C without address conflict. However, the I2C ID addresses of all the peripheral parts for FT3C02 are defined. Users have to configure the ID addresses of those parts in the PCB design stage.

I2C	Bus Device Name	I2C Device Address	Remark
Host	NS3D0s	0b 010.0100 0b 010.0101 0b 010.0110 0b 010.0111	Configurable
Peripheral	EEPROM (Atmel AT24C128C or compatible)	0b 101.0000	Must be fixed
	EEPROM (inside provisioned MCLK OCXO-CC module P/N)	0b 101.0100	Must be fixed
	Temperature Sensor (TI TMP116/117)		
	Temperature Sensor (AMS AS621X)	0b 100.1000	Must be fixed
	Temperature Sensor (inside provisioned MCLK OCXO-CC module P/N)		

FT3C02 Host I2C Interface, the I2C Frame and Data Transfer Format

Pins I2C_IDO and I2C_IDO1 enable the user to have multiple FT3C02 ICs on the same I2C bus. The device address of the host I2C interface could be 0b010.01ab, where "a" is configured by pin I2C_ID1 and "b" is configured by pin I2C_ID0 (high=1; low=0). The I2C ID address could be configured in either PCB circuit design stage or on the BOM (bill of material) stage.

The user host controller (micro-controller or FPGA) could have register reading and writing to access and manipulate FT3C02. It supports a 7-bit I2C ID address. The format is MSB-bit (most significant bit) leading. The format uses only one byte for 8-bit register address. For read/write multiple bytes in burst mode, the register address will be increased by one automatically for each data byte.

Abbreviations
- A: Acknowledge
- $\overline{A}$: No acknowledge
- S: Start
- P: Stop
- R: Read
- W: Write
- Sr: Repeated Start

Host I2C Frame Format

Write Format

Single Byte

S	ID[6:0]	W	A	ADR[7:0]	A	WDATA[7:0]	A	P

Multiple Bytes

S	ID[6:0]	W	A	ADR[7:0]	A	WDATA1[7:0]	A	WDATA2[7:0]	A	P

Read Format 1

Single Byte

S	ID[6:0]	W	A	ADR[7:0]	A	Sr	ID[6:0]	R	A	RDATA[7:0]	$\overline{A}$	P

Multiple Bytes

S	ID[6:0]	W	A	ADR[7:0]	A	Sr	ID{6:0}	R	A	RDATA1[7:0]	A	RDATA2[7:0]	$\overline{A}$	P

Read Format 2

Single Byte

S	ID[6:0]	W	A	ADR[7:0]	A	P
S	ID[6:0]	R	A	RDATA1[7:0]	$\overline{A}$	P

Multiple Bytes

S	ID[6:0]	W	A	ADR[7:0]	A	P
S	ID[6:0]	R	A	RDATA1[7:0]	A	RDATA2[7:0]	A	P

Multiple-Byte Register Read/Write Data Format

FT3C02's registers are either single-byte or multiple-byte registers. For multiple-byte registers, the reading/writing sequence is to start from the LSB (least significant byte) byte to the MSB (most significant byte) byte, without any other read/write interrupt. The LSB byte of a multiple-byte registers always have the lower address. The timeout of each multiple-byte reading is around 100 mini seconds. The writing of the multiple bytes will take affect after the MSB byte writing.

Internal OTP/MTP and External EEPROM

The Internal OTP/MTP

FT3C02 has an internal OTP of 13,696 byte size. The first 13,312 bytes store the firmware image used by FT3C02's proprietary embedded ALU. This image will be pre-programmed by the manufacturer before shipping. The other 384 bytes could be used as multiple-time programming storage, split into six 64-byte segment of MTPs, to carry the TEMPCO (temperature coefficients) table for the automatic thermal frequency offset projection. The format of the TEMPCO table will be illustrated in a later section.

The External EEPROM

FT3C02 can work with an external field upgrade EEPROM to carry the update firmware and the customized register initial values. It could also piggyback carry the TEMPCO Set for automatic thermal frequency offset projection. This EEPROM, being either ATMEL's AT24C128C or its compatible products with I2C ID address of 0b101.0000, has to be placed on the Peripheral I2C bus via pins MSDA and MSCL.

The first 13,504 bytes on the EEPROM will store the update firmware and the customized register initial values. Its first 13,312 bytes are for the update firmware and the following 160 bytes are the initial values of the registers of address from 0x00 to 0x9F. Only write-able registers' values will be initialized by the content here. The next 28 bytes are not used, followed by two byte of magic key 0x55 and 0xAA, and then the last two bytes for CRC16 checksum. The CRC16 checksum covers the previous 13,502-byte content, using MSB-bit-leading CRC16 checksum algorithm with CRC16 polynomial (X16) + X15 + X2 + X0.

Then the first 64 bytes of the leftover 2880 bytes could be used to piggyback store the TEMPCO Set for automatic thermal frequency offset prediction.

Every time FT3C02 was booted up from soft reset (see register SOFT_RESET) or from power on, FT3C02 will load from its internal OTP first, then it will check the existence of the external EEPROM. If the EEPROM exists and the content of its bytes 13,500 and 13,501 match the magic keys, the update firmware and the register initial values will be downloaded to override the content from OTP.

FT3C02 Detailed Register Table

ADDR	BITS	REGISTER NAME	I/O	DEFAULT	DESCRIPTION
0x00	[7:0]	Chip_ID Byte 0	R	0x46	Chip ID, byte 0: ASCII code of 'F'
0x01	[7:0]	Chip_ID Byte 1	R	0X54	Chip ID, byte 1: ASCII code of 'T'
0x02	[7:0]	Chip_ID Byte 2	R	0x33	Chip ID, byte 2: ASCII code of '3'
0x03	[7:0]	Chip_ID Byte 3	R	0x43	Chip ID, byte 3: ASCII code of 'C'
0x04	[7:0]	Chip_ID Byte 4	R	0x30	Chip ID, byte 4: ASCII code of '0'
0x05 [	7:0]	Chip_ID Byte 5	R	0x32	Chip ID, byte 5: ASCII code of '2'
0x06	[7:0]	Chip_ID Byte 6	R	0x00	Chip ID, byte 6: ASCII code of '\0'
0x07	[7:0]	Chip_REV	R	1	Chip Revision of FT-3C02_Rev_1.1
0x08	[7:0]	FW_REV	R	1	Firmware Revision of FT-3C02_Rev_1.1
0x10	[7:0]	APLL_REF_FREQ	r/W	0	The frequency of APLL's reference clock synthesized from NPLL. FREQ = reg_value x 8kHz **reg_value must be in the range from 5 to 125**
0x11	[13:0]	APLL_FB_DIV	r/W	0	APLL's 14-bit feedback divider; reg_value==0 means disable
0x13	[0]	APLL_R0_CHOICE	r/W	0	APLL's R0 choice, 0 Selection of R0 using register APLL_R0_VALUE_L 1 Selection of R0 using register APLL_R0_VALUE_S
0x14	[8:0]	APLL_R0_VALUE_L	r/W	0	APLL's R0_VALUE_L resistance selection. Unit in ohm. bit[0] RL[0]; 0: 1k, 1: 10k bit[1] RL[1]; 0: 1k, 1: 20k bit[2] RL[2]; 0: 1k, 1: 40k bit[3] RL[3]; 0: 1k, 1: 80k bit[4] RL[4]; 0: 1k, 1: 160k bit[5] RL[5]; 0: 1k, 1: 320k bit[6] RL[6]; 0: 1k, 1: 640k bit[7] RL[7]; 0: 1k, 1: 1280k bit[8] RL[8]; 0: 1k, 1: 2560k R0_VALUE_L = RL[0] + RL[1] + … RL[7] + RL[8]
0x16	[4:0]	APLL_R0_VALUE_S	r/W	0	APLL's R0_VALUE_S resistance selection. Unit in ohm. bit[0] Rs[0]; 0: 0.4k, 1: 2.5k bit[1] Rs[1]; 0: 0.4k, 1: 5k bit[2] Rs[2]; 0: 0.4k, 1: 10k bit[3] Rs[3]; 0: 0.4k, 1: 20k bit[4] Rs[4]; 0: 0.4k, 1: 40k R0_VALUE_S = Rs[0] + Rs[1] + Rs[2] + Rs[3] + Rs[4]
0x17	[3:0]	APLL_R2_DIV	r/W	0	APLL's R2 resistance = (160k ohm) / reg_value; **This value must NOT be 0.**
0x18	[11:0]	APLL_CP_CURRENCY	r/W	0	APLL's charge pump currency = 0.3125uA * reg_value
0x1A	[7:0]	TEST_MODE1	r/W	0	TEST MODE1 (for internal use only). MUST BE 0
0x1B	[7:0]	TEST_MODE2	r/W	0	TEST MODE2 (for internal use only). MUST BE 0
0x1C	[7:0]	TEST_MODE3	r/W	4	TEST MODE3 (for internal use only). MUST BE 4
0x20	[1:0]	MCLK_TEMPCO_SRC	r/W	0	The source selection of the Temperature Coefficient for automatic MCLK temperature compensation calculation 0: internal OTP The image content format will be illustrated later. 1: external I2C EEPROM (ATMEL AT24C128C or compatible The image content format will be illustrated later. 2,3: external I2C EEPROM inside CW OH20TSE-010.0M)

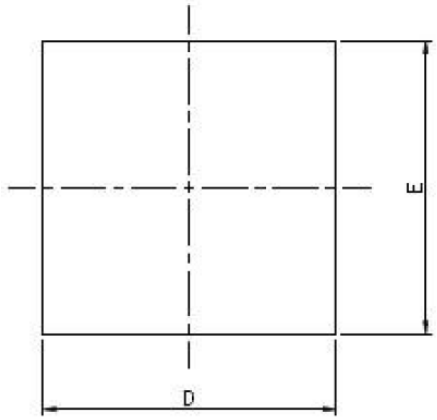
FT3C02 Detailed Register Table continued

ADDR	BITS	REGISTER NAME	I/O	DEFAULT	DESCRIPTION
0x21	[0]	MCLK_TEMP_SENSOR_TYPE	r/W	0	The type of the temperature sensor used for automatic MCLK temperature compensation 0: TI TMP116/117, or compatible 1: AMS AS621X, or compatible
0x22	[0]	MCLK_AUTO_TEMP_ADJ_REVERSE	r/W	0	The reverse the positive/negative polarity of calculation result of the automatic MCLK temperature compensation. 0: No reverse 1: to reverse
0x40	[5:0]	OUT1_POST_DIV	r/W	1	The post divider of OUT1, 6-bit; 0: disable
0x41	[13:0]	OUT2_POST_DIV	r/W	0	The post divider of OUT2, 14-bit; 0,1: disable
0x43	[31:0]	MCLK_USER_ADJ	r/W	0	The MCLK extra user adjustment, unit in (ppb/1024), 2's complement
0x47	[0]	MCLK_USE_AUTO_TEMP_ADJ	r/W	0	To specify whether using automatic MCLK temperature compensation calculation result 0: no 1: Yes
0x48	[1:0]	MCLK_TEMP_SENSOR_RATE	r/W	0	Temperature Sensor Reading Rate for automatic MCLK temperature compensation 0: OFF 1: 1 time/sec 2: 2 times/sec 3: 4 times/sec FT3C02 will communicate with the external temperature sensor to change its conversion cycle time and the average configuration automatically. Users do not need to communicate to the temperature sensor directly.
0x50	[15:0]	MCLK_TEMP_SENSOR_VALUE	R		The raw value read from the temperature sensor for the automatic MCLK Temperature compensation
0x52	[31:0]	MCLK_AUTO_TEMP_ADJ_RESULT	R		The calculation result of the automatic MCLK temperature compensation, unit in (ppb/1024), 2's comp. <PS> Whether this calculation result will be applied to MCLK calibration depends on register MCLK_USE_AUTO_ADJ.
0x56	[31:0]	MCLK_TOTAL_ADJ	R		The total MCLK adjustment, unit in (ppb/1024), 2's complement
0x80	[7:0]	MCLK_TEMPCO_PAGE_IDX	R		The EEPROM page index of the found Temperature Coefficient. The valid page index is from 214 to 255. Value other than these indicates no valid data found.
0xA0	[5:0]	LOAD_STATUS	R		LOAD status bit[0] load complete; 0: not completed, 1: completed bit[1] OTP content; 0: invalid, 1: valid bit[2] ~RSVD~ bit[3] EEPROM existence; 0: non-detected, 1: detected Bit[4] EEPROM content; 0: invalid, 1: valid bit[5] EEPROM content checksum; 0: FAILED, 1: SUCC

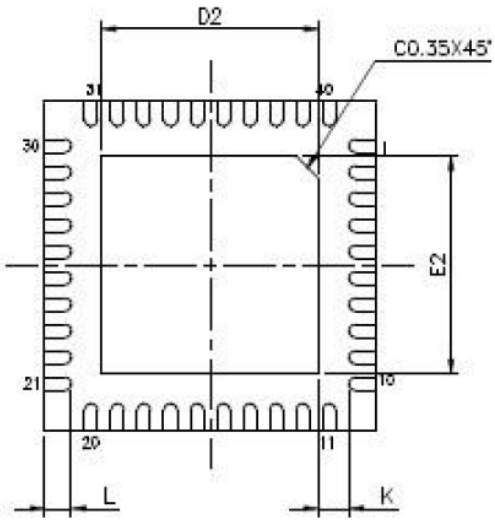
FT3C02 Detailed Register Table continued

ADDR	BITS	REGISTER NAME	I/O	DEFAULT	DESCRIPTION
0xA1	[7:0]	EEP/OTP_PAGE_IDX	r/W	0	To specify the page index of EEPROM/OTP to read from or write to
0xA2	[0]	EEPROM_CMD	W		EEPROM command to start the page reading or writing of a 64-byte page data • Write 0 to initiate the 64-byte writing from the REGS (PAGE_BUFFER) to the EEPROM page specified by REG(EE/OTP_PAGE_IDX). • Write 1 to initiate the 64-byte reading from the EEPROM page specified by REG(EE/OTP_PAGE_IDX) to the REGS(PAGE_BUFFER).
	[2:0]	EPROM_STS	R		The status of the EEPROM bit[0] 0: WRITE, 1: READ bit[1] 0: ready, 1: not ready bit[2] 0: EEPROM exists, 1: EEPROM not exists
0xA3	[7:0]	SOFT_RESET	W		IC Soft Reset write value 0xA5 to reset the IC
0xA4	[0]	OTP_CMD	W		OTP command to start the page reading of writing of a 64-byte page data • Write 0 to initiate the 64-byte writing from the REGS(PAGE_BUFFER) to the OTP page specified by REG(EE/OTP_PAGE_IDX). • Write 1 to initiate the 64-byte reading from the OTP page specified by REG(EE/OTP_PAGE_IDX) to the REGS(PAGE_BUFFER).
	[1:0]	OTP_STS	R		The status of the OTP bit[0] 0: WRITE, 1: READ bit[1] 0: ready, 1: not ready
0xA5	[11:0]	OTP_PWE_TIMER	r/W		The time to program one byte on OTP, unit in internal clock cycle; For FT-3C02, set the value to be 2333
0xA7	[0]	Peripheral_I2C_BUS_STS	R		The status of Peripheral I2C bus 0: IDLE 1: BUSY <ps> This Peripheral I2C bus is the I2C bus to the EEPROM, Temp_Sensor, and Connor-Winfield OH320-CC. FT-3C02 is the master controller of this I2C bus.
0xC0~0xFF	64 x [7:0]	PAGE_BUFFER	R/W		The 64-byte page buffer for OTP/EEPROM page read/write operation Instead of using FIFO, FT-3C02's page buffer is a 64-byte wide random access buffer.

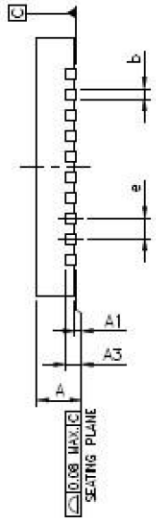
FT3C02 Package Dimensions



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		5.00 BASIC	
E		5.00 BASIC	
e		0.40 BASIC	
K	0.20	—	—

PAD SIZE (MIL)	MILLIMETER					
	D2/E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
159X159-G	3.74	3.79	3.84	0.25	0.30	0.35

Revision History

Revision	Date	Note
00	08/23/23	New Release

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