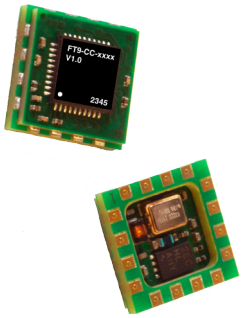
DATA SHEET

FT9-CC
Self Compensating Frequency translator

Overview



The FT9-CC is a highly integrated clock frequency translation module designed to receive a 10MHz reference input and generate up to two frequency-translated single-ended clock outputs phase locked to the incoming 10MHz signal. This high precision phase and frequency synchronization solution supports low phase noise frequency clock translation with its on-board fundamental frequency VCXO.

The FT9-CC supports virtually any 10 MHz 3.3V clock signal as the input to the module for translating to the output frequency. However, the primary feature of the FT9-CC is in its auto-calibration function used to calibrate and correct for frequency offsets to compensate for thermal drift found in a specially provisioned external supporting OCXO and TCXO models. Using pre-programmed Temperature Sense Enabled (TSE) clock modules, the FT9-CC can automatically read temperature sensor values and auto calculate the TSE module's thermal instability to compensate the TSE module's thermal drift without the need for an external micro controller. An OCXO TSE module can be compensated to ±0.3ppb over the specified operating temperature range. An internal disciplined VCXO provides the output characteristics for phase noise and jitter performance for the two single ended clock outputs with excellent jitter performance at frequencies up to 156.25MHz, which can be further divided down at the output ports with 6- and 14-bit divider values.

This product can be used to support a high-stability frequency reference for use in wireless systems, IEEE 1588v2, and any application that requires frequency translation.

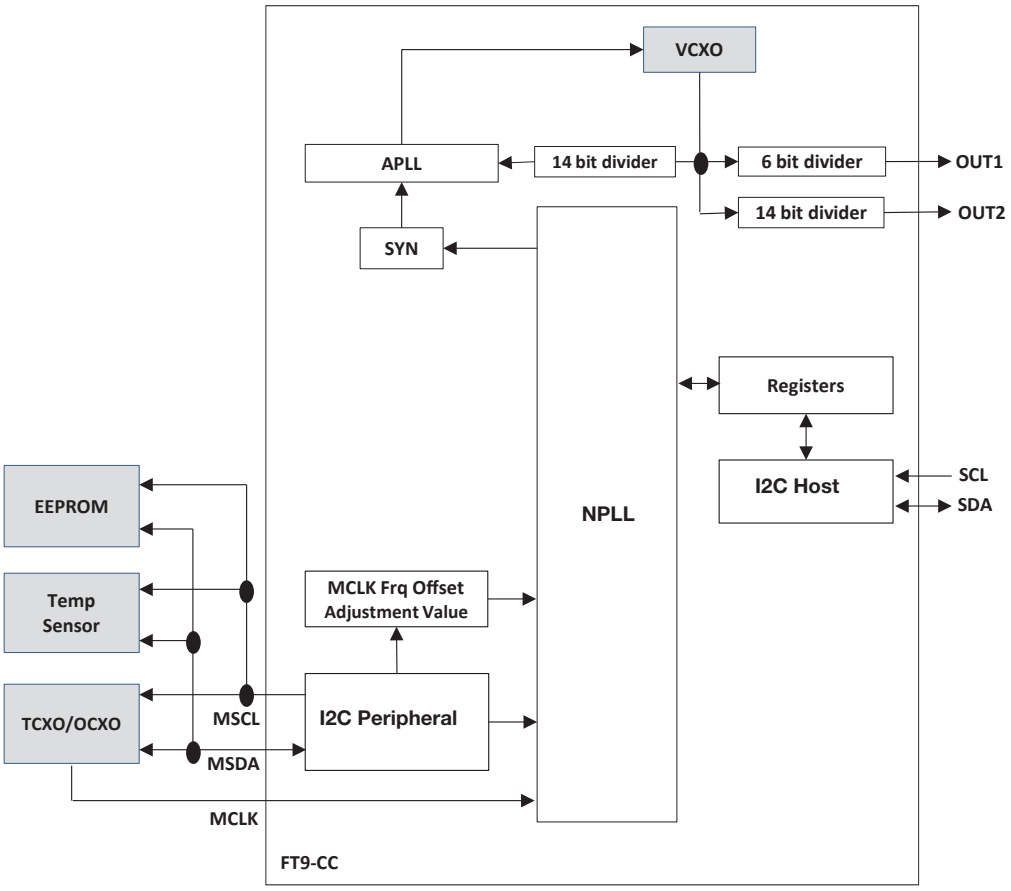
Features

- Phase locks to an incoming 10 MHz Master Clock input
- Generates up to two (2) single ended Low Jitter Clock Outputs derived from internal VCXO
- Internal VCXO supports up to 156.25 MHz clock output frequency range
- 6-bit and 14-bit output dividers from internal VCXO frequency
- Automatic compensation of external correctable Temp Sense Enabled (TSE) modules
- I2C Interface for system communication.
- 3.3VDC Supply Voltage
- -40°C to 105°C operating temperature range
- 9.2 x 9.2mm 16 pin QFN surface mount package

Applications

- High Stability Clocking
- Primary Reference Time Clock (PRTC) [G.8272]
- Telecom Grand Master [G.8273.1]
- Telecom boundary clock [G.8273.2]
- Wireless Base Stations
- GNSS Disciplined Oscillator
- NTP Stratum 0 Standard

FT9-CC Functional Block Diagram



Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	125	°C	
Supply Voltage	-0.5	-	4.5	Vdc	
Operating Supply Voltage 3.3 Vdc	3.13	3.30	3.47	Vdc	

Absolute Ratings: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only. The functional operation of the device at those or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to conditions outside the "recommended operating conditions" for any extended period of time may adversely impact device reliability and result in failures not covered by warranty.

Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Supply Voltage (AVDD33, DVDD33)	3.13	3.30	3.47	Vdc	
Supply Current		125	150	mA	
Operating Temperature Range	-40	-	105	°C	

LVCMOS Output Characteristics

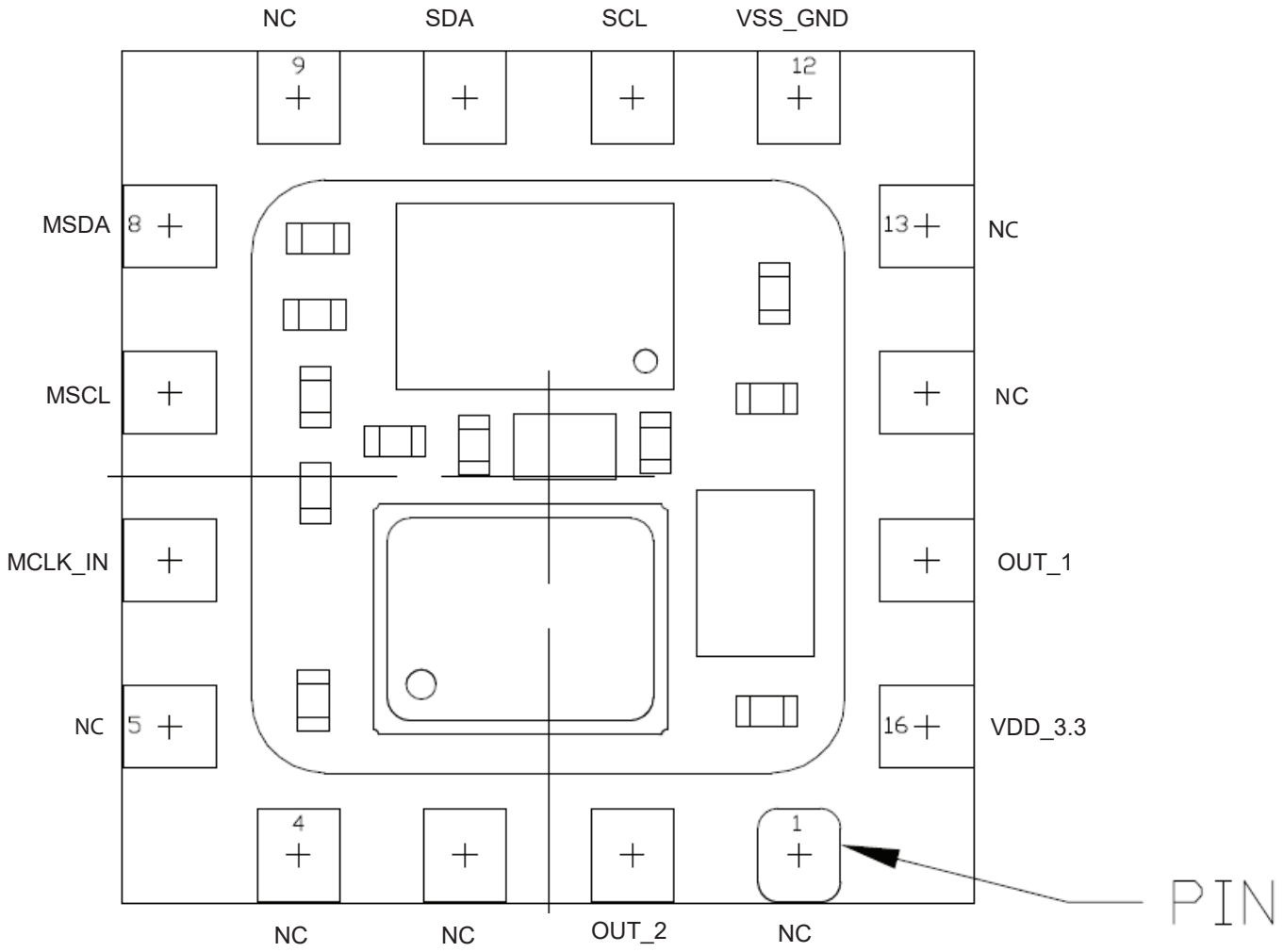
Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	15	-	pF	
Output Voltage					
(High) (Voh)	3.0	-	-	V	
(Low) (Vol)	-	-	0.4		
Duty Cycle at 50% of Vcc	45	50	55	%	1
	35	40	45	%	2
Rise / Fall Time 10% to 90%	-	-	6	ns	

Package Characteristics

Package	9.2 x 9.2mm 16 pin QFN
Moisture Sensitivity Level	MSL-3

1) Applies when OUTx_POST_DIV is set to 1 or any even number.
2) Applies when OUTx_POST_DIV is set to an odd number greater than 1.

FT9-CC Pin Assignments (Bottom View)



FT9-CC Pin Description

Pin No.	Pin Name	I/O	Description
1	NC		
2	OUT_2	O	3.3V LVCMOS Output
3	NC		
4	NC		
5	NC		
6	MCLK_IN	I	Master Clock input. Accepts 3.3V LVCMOS clock signal input
7	MSCL	I/O	Peripheral Series Clock Output, Communications with data from Temp Sensor
8	MSDA	I/O	Peripheral Series Data. Accepts data from Temp Sensor
9	NC		
10	SDA	I/O	HOST I2C Series Data
11	SCL	I/O	HOST I2C Series Clock Putput
12	VSS_GND	Power	GROUND
13	NC		
14	NC		
15	OUT_1	O	3.3V LVCMOS Output
16	VDD_3.3	Power	3.3V Power Input

General Description

The FT9-CC module is designed to receive a 10MHz master clock input and generate up to two frequency-translated single-ended clock outputs phase locked to the incoming 10MHz signal. The FT9-CC supports virtually any 10.00 MHz 3.3V clock signal as the input to the module for translating to the output frequency. However, the primary feature of the FT9-CC is in its auto-calibration function used to calibrate and correct for frequency offsets to compensate for thermal drift found in specially provisioned external supporting OCXO and TCXO MCLK modules. Using pre-programmed Temperature Sense Enabled (TSE) clock modules, the FT9-CC can automatically read temperature sensor values and auto calculate the TSE module's thermal instability to compensate the TSE module's thermal drift without the need for an external micro controller. A TSE OCXO module can be compensated to ±.3ppb over the specified operating temperature range.

The analog portion of the chip consists of an independent APLL circuit with integrated charge pump and phase detector, supported by an internal VCXO, that translates the 10 MHz frequency and attenuates the jitter on the synthesized clock output generated in the NPLL section of the chip. Two single ended output clocks are derived from the disciplined VCXO. The internal VCXO used provides the output characteristics for phase noise and jitter performance for the 2 clock outputs. The two LVCMOS level clock output transmitters OUT_1 and OUT_2 have follow-on divider circuits available. Output 1 has a 6-bit divider capability, while output 2 has a 14-bit divider capability.

The FT9-CC has functionality for creating frequency offsets in its internal master clock that allows for a compensation scheme to support ultra-high stability enhancement in applications where high precision holdover performance is required. A peripheral I2C connection supports direct communication with OCXO modules enabled with compatible TSE circuitry. The FT9-CC can also be controlled externally via micro-controller to access its numerical frequency offset calibration to a resolution of less than 1 part per trillion. This provides the user an ability to enhance the frequency stability of the internal MCLK input beyond its naked external MLCK source, including compensating for aging as well as initial calibration frequency offset.

The module is configured at the factory based on the internal VCXO frequency chosen; however, certain registers in the module can be accessed through the module's I2C pins allowing the user to make various adjustments These adjustments allow the user to:

1. Change the register value on each of the two output port post dividers
2. Change the read rate of the internal temperature sensor
3. Make adjustments to the internal user specified calibrated adjustment register
4. Turn on/off the auto calibration function
5. Initiate a soft reset

Through the I2C connection, the user can also read information on the internal operation of the systems including:

1. Read the raw temperature sensor value
2. Read the compensation calculation result
3. Read the MCLK total frequency offset adjustment value

FT9-CC Module Register Table

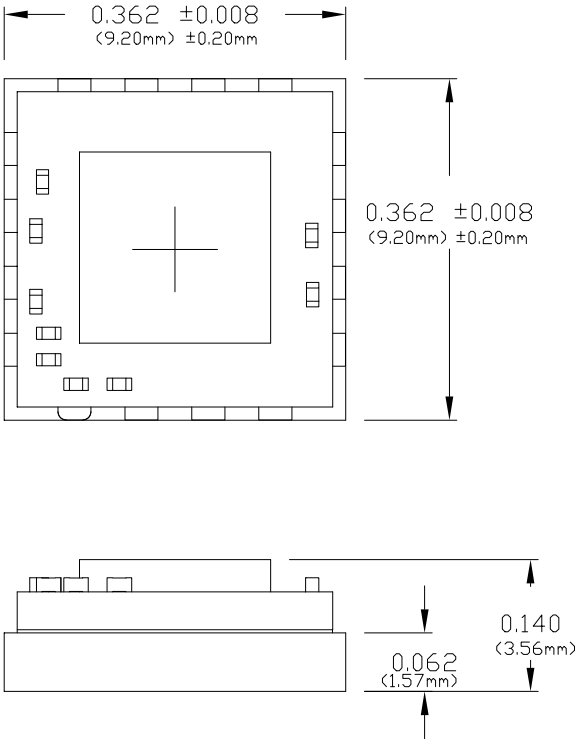
I/O Description: R = Read Only; W = Write Only; r/W = Write, but previous written value could be read back; R/W = Read and Write

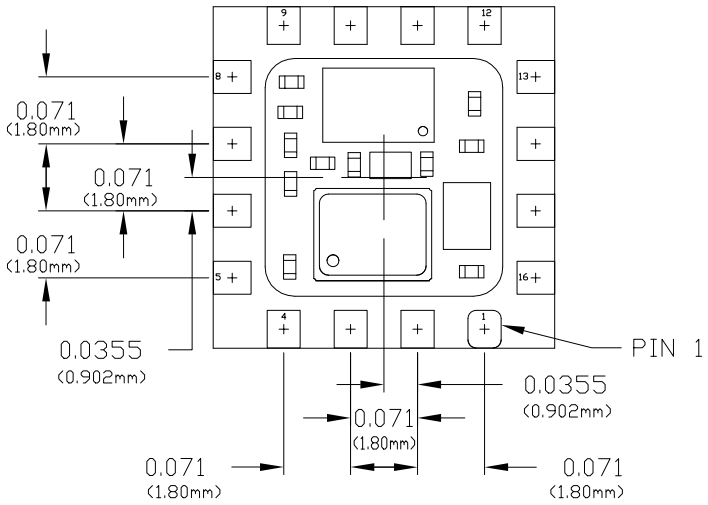
ADDR	BITS	REGISTER NAME	I/O	DESCRIPTION
0x00~0x06	7 x [7:0]	Chip_ID	R	Chip ID, from byte #0 to byte #6
0x07	[7:0]	Chip_REV	R	Chip Revision
0x08	[7:0]	FW_REV	R	Firmware Revision
0x09~0x3F				~RSVD~
0x40	[5:0]	OUT1_POST_DIV	r/W	OUT1 Post Divider
0x41	[13:0]	OUT2_POST_DIV	r/W	OUT2 Post Divider
0x43	[31:0]	MCLK_USER_ADJ	r/W	User specified MCLK adjustment
0x47	[0]	MCLK_USE_AUTO_TEMP_ADJ	r/W	Selection of using automatic MCLK temperature compensation calculation
0x48	[1:0]	MCLK_TEMP_SENSOR_RATE	r/W	Temperature Sensor Reading Rate
0x49~0x4F				~NOT USED~
0x50	[15:0]	MCLK_TEMP_SENSOR_VALUE	R	MCLK Temperature Sensor Raw Reading
0x52	[31:0]	MCLK_AUTO_TEMP_ADJ_RESULT	R	MCLK Temperature Compensation Calculation Result
0x56	[31:0]	MCLK_TOTAL_ADJ	R	MCLK total adjustment
0x5A~0x7F				~NOT USED~
0x80	[7:0]	MCLK_TEMPCO_PAGE_IDX	R	EEPROM Page Index of found MCLK Temperature Coefficients
0x81~0x9F				~RSVD~
0xA0	[5:0]	LOAD_STATUS	R	EEPROM load status
0xA1	[7:0]	EEPROM_PAGE_IDX	r/W	Target EEPROM read/write page index
0xA2	[0]	EEPROM_CMD	W	EEPROM command
	[2:0]	EEPROM_STS	R	EEPROM status
0xA3	[7:0]	SOFT_RESET	W	IC Soft Reset Command
0xA4~0xBF				~RSVD~
0xC0~0xFF	64 x [7:0]	PAGE_BUFFER	R/W	EEPROM read/write page buffer, from byte#0 to byte#63

FT9-CC Module Register Detailed Description

ADDR	BITS	REGISTER NAME	I/O	Value	DESCRIPTION
0x00	[7:0]	Chip_ID Byte 0	R	0x46	Chip ID, byte 0: ASCII code of 'F'
0x01	[7:0]	Chip_ID Byte 1	R	0X54	Chip ID, byte 1: ASCII code of 'T'
0x02	[7:0]	Chip_ID Byte 2	R	0x33	Chip ID, byte 2: ASCII code of '3'
0x03	[7:0]	Chip_ID Byte 3	R	0x43	Chip ID, byte 3: ASCII code of 'C'
0x04	[7:0]	Chip_ID Byte 4	R	0x30	Chip ID, byte 4: ASCII code of '0'
0x05	[7:0]	Chip_ID Byte 5	R	0x32	Chip ID, byte 5: ASCII code of '2'
0x06	[7:0]	Chip_ID Byte 6	R	0x00	Chip ID, byte 6: ASCII code of '\0'
0x07	[7:0]	Chip_REV	R	1	Chip Revision
0x08	[7:0]	FW_REV	R	1	Firmware Revision
0x40	[5:0]	OUT1_POST_DIV	r/W	1	The post divider of OUT1, 6-bit; 0: disable
0x41	[13:0]	OUT2_POST_DIV	r/W	0	The post divider of OUT2, 14-bit; 0,1: disable
0x43	[31:0]	MCLK_USER_ADJ	r/W	0	The MCLK extra user adjustment, unit in (ppb/1024), 2'scomplement
0x47	[0]	MCLK_USE_AUTO_TEMP_ADJ	r/W	0	To specify whether using automatic MCLK temperature compensation calculation result 0: no 1: Yes
0x48	[1:0]	MCLK_TEMP_SENSOR_RATE	r/W	0	Temperature Sensor Reading Rate for automatic MCLK temperature compensation 0: OFF 1: 1 time/sec 2: 2 times/sec 3: 4 times/sec FT9-CC will communicate with the external temperature sensor to change its conversion cycle time and the average configuration automatically. Users do not need to communicate to the temperature sensor directly.
0x50	[15:0]	MCLK_TEMP_SENSOR_VALUE	R		The raw value read from the temperature sensor for the automatic MCLK Temperature compensation
0x52	[31:0]	MCLK_AUTO_TEMP_ADJ_RESULT	R		The calculation result of the automatic MCLK temperature compensation, unit in (ppb/1024), 2's comp. <PS> Whether this calculation result will be applied to MCLK calibration depends on register MCLK_USE_AUTO_ADJ.
0x56	[31:0]	MCLK_TOTAL_ADJ	R		The total MCLK adjustment, unit in (ppb/1024), 2's complement
0xA0	[5:0]	LOAD_STATUS	R		LOAD status bit[2:0] ~RSVD~ bit[3] EEPROM existence; 0: non-detected, 1: detected bit[4] EEPROM content; 0: invalid, 1: valid bit[5] ~RSVD~
0xA1	[7:0]	EE_PAGE_IDX	r/W	0	To specify the page index of EEPROM to read from or write to
0xA2	[0]	EEPROM_CMD	W		EEPROM command to start the page reading or writing of a 64-byte page data • Write 0 to initiate the 64-byte writing from the REGS(PAGE_BUFFER) to the EEPROM page specified by REG(EE_PAGE_IDX). • Write 1 to initiate the 64-byte reading from the EEPROM page specified by REG(EE_PAGE_IDX) to the REGS(PAGE_BUFFER).
	[2:0]	EEPROM_STS	R		The status of the EEPROM bit[0] 0: WRITE, 1: READ bit[1] 0: ready, 1: not ready bit[2] 0: EEPROM exists, 1: EEPROM not exists
0xA3	[7:0]	SOFT_RESET	W		IC Soft Reset write value 0xA5 to reset the IC
0xC0~0xFF	64 x [7:0]	PAGE_BUFFER	R/W		The 64-byte page buffer for EEPROM page read/write operation Instead of using FIFO page buffer is a 64-byte wide random access buffer.

FT9-CC Mechanical Drawing

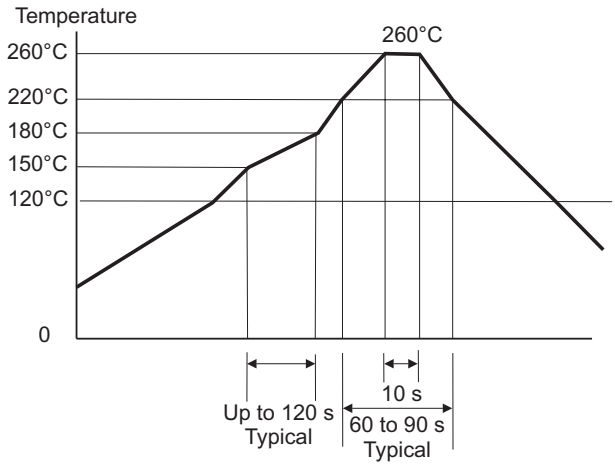




(BOTTOM VIEW)

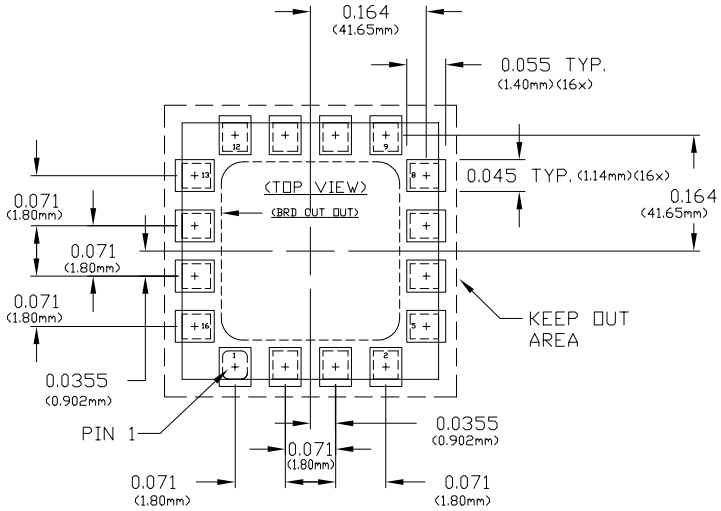
Dimensional Tolerance:
±0.005 (±0.127mm) unless shown otherwise

Solder Profile



Meets IPC/JEDEC J-STD-020C

Suggested Pad Layout



KEEP OUT AREA
UNDER THE PCBOARD IS A KEEP OUT AREA,
DO NOT PLACE ANY PARTS IN THIS AREA.

Standard Frequencies

10.00 MHz	A		
100.00 MHz	B	65.5360 MHz	T
122.88 MHz	C	32.768 MHz	W
125.00 MHz	D	64.0 MHz	X
156.25 MHz	E	38.880 MHz	Y
80 MHz	F	51.84 MHz	Z
98.304 MHz	G		
61.44 MHz	H	16.384 MHz	0
77.76 MHz	J	30.72 MHz	1
155.520 MHz	K	20.48 MHz	2
50 MHz	L	5.0 MHz	3
64 MHz	M	12.8 MHz	4
40 MHz	N	49.152 MHz	5
20.0 MHz	O	16.0 MHz	6
25.0 MHz	P	19.440 MHz	7
96.0 MHz	R	10.24 MHz	8
81.92 MHz	S	8 kHz	9

Ordering Information

FT9-CC- [X] [X] [X] [X]

Output Frequency 2 See standard frequencies chart above. * If the desired frequency is not listed, Please Consult a sales representative for availabilty of additional frequencies.

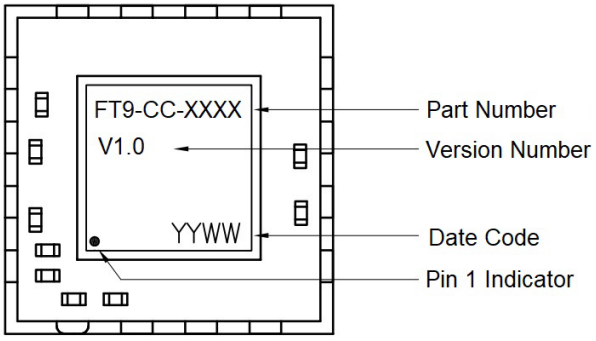
OUTPUT **Frequency** 1
See standard frequencies chart above.

Number of Output Frequencies
1: 1 Output Frequency
2: 2 Output Frequencies

VCXO Frequency - See standard frequencies chart above.

Example Part Number: FT9-CC-2BAP

Marking Configuration



Revision History

Revision	Date	Note
00	08/30/23	New Release
01	12/28/23	Added marking configuration, updated photo and supply current specification.
02	02/15/24	Added duty cycle variation when dividing by odd numbers

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