NTC1012
Zero Delay Clock Buffer with PWM Message Forwarding

DATA SHEET

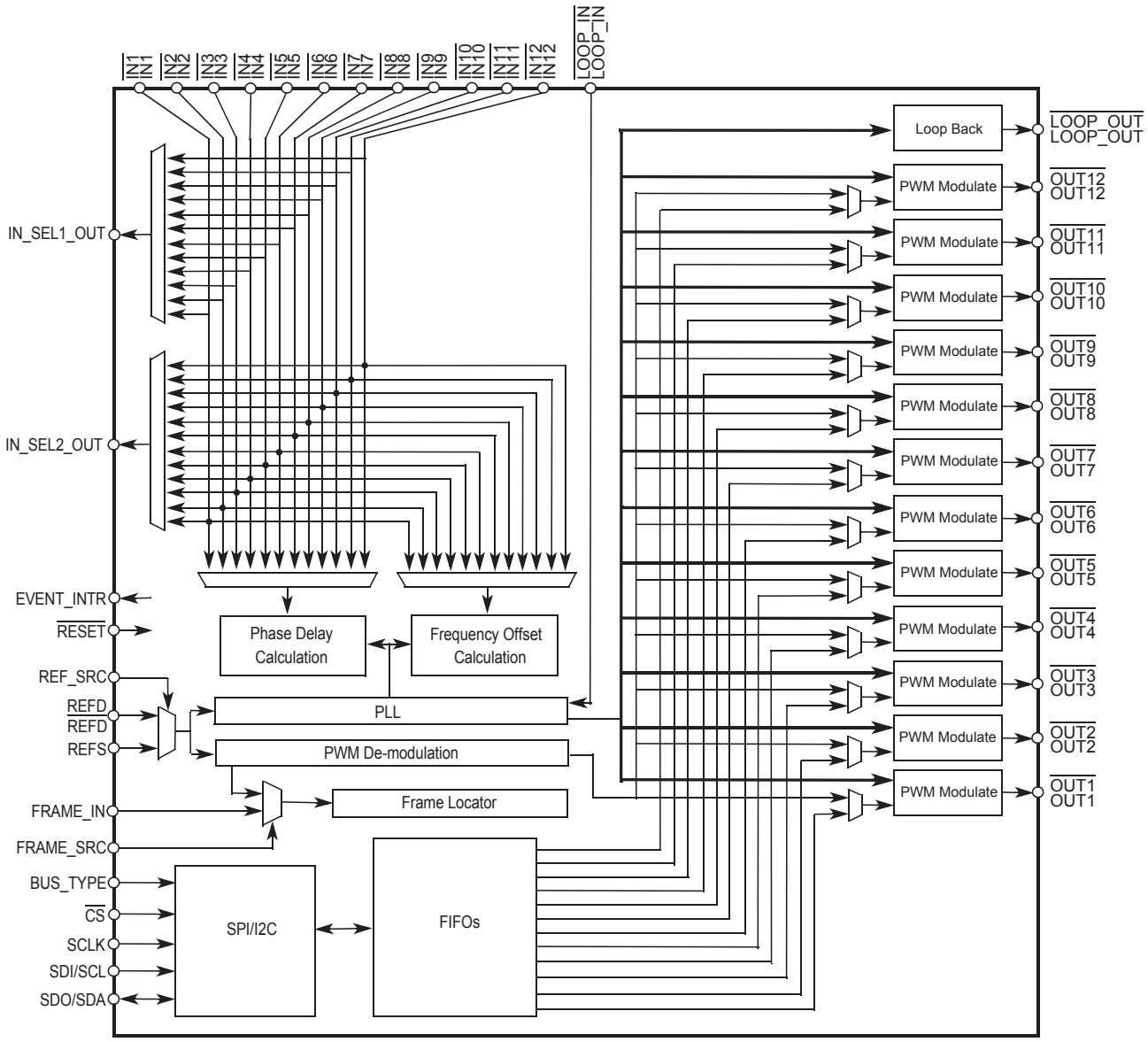
Overview

The NTC1012 is a highly integrated multi-function synchronizing IC. It combines the functionality of a low jitter, zero delay clock buffer, a multi output clock generator, an integrated pulse width modulation (PWM) messaging capability and an internal phase detector. The source of the PWM message transmitted onto the output clock signals can be chosen from either of two options: the de-modulation of a PWM message on the incoming reference clock or written directly from data generated and supplied by the user. The NTC1012 allows the user to calculate and compare both phase delay as well as the frequency offset between a source reference and one of 12 inputs (IN1 - IN12). Two of the 12 differential inputs can be selected independently and converted to two single-ended outputs to support the phase and frequency offset measurement and comparison.

The NTC1012 provides twelve 3.3V LVDS output ports (OUT1 – OUT12) that generate clock signals that are phase locked and phase aligned with the reference input. One of the rising edges of the reference clock is used to identify the SYNC position, which is also the position to begin sending PWM data. This position can be determined from either the FRAME_IN signal or from PWM data carried by the reference clock. The NTC1012 is capable of either de-modulating a formatted PWM message modulated onto the 25MHzor 10MHz input reference or using the data supplied by user to modulate a PWM message onto each of the twelve output signals.

Twelve LVDS output transmitter ports each have a dedicated FIFO to store user supplied data allowing the final output PWM message to be generated from either the dedicated FIFO or from the de-modulated PWM message obtained from the reference input. The user can individually control the message within each FIFO/output or send a global message to all twelve outputs at once. Communication and interrogation of system activity is available through either I2C or SPI bus interfaces.

NTC1012 Functional Port Diagram



Specifications

Parameter	Specification
Voltage	3.3V ±5% and 1.8Vdc ±5%
Power	20-30 mA per LVDS output depending on signal amplitude
Temperature	-40 to 85°C Industrial temp range operation
Frame Reference Frequency	1, 2, 4 kHz or 8 kHz
XI/XO Input	Single ended clock signal or fundamental mode crystal
REF_IN/Output Frequency Options	25 MHz or 10 MHz
Dimensions	14x 14 x 1.4 mm 128 pin LQFP package

NTC1012 General Description

The NTC1012 is a highly integrated multi-function synchronizing IC. It combines the functionality of a low jitter zero delay clock buffer, a multi output clock generator, an integrated pulse width modulation (PWM) messaging capability, an internal phase detector to support the measurement of phase delay and fractional frequency offset calculation and generation of two single-ended outputs selected from the 12 differential inputs (In_1-In_12). The NTC1012 offers five primary functions:

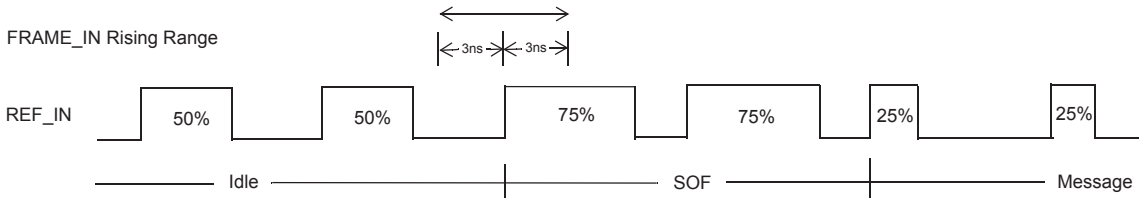
Zero-Delay Clock Buffer

The NTC1012 requires an external loop back clock to achieve its zero-delay clock buffer requirement. The output of LOOP_OUT should be connected to LOOP_IN externally. An internal PLL locks onto the 25MHZ REF_IN reference and compares the phase difference between the input of FRAME_IN and LOOP_IN. It then adjusts the phase of LOOP_OUT and outputs OUT1 - OUT12 globally to maintain the minimum phase skew between FRAME_IN and all output signals. The skew can also be programmatically controlled.

The 25MHz REF_IN clock may contain a PWM message that can be forwarded to each or all output ports. If the PWM message needs to be de-modulated and modulated onto any output ports, the rising edge of SOF (start of frame) clock cycle at REF_IN need to be aligned with the rising edge of FRAME_IN within +-3ns as shown in Fig 2. The SOF is two 75% high time clock cycles after a 50% duty (idle cycle) clock cycle from REF_IN. If none of the outputs need to carry PWM message from REF_IN, the phase relation of REF_IN and FRAME_IN can be arbitrary

REF_IN with PWM and FRAME_IN Relation

Figure 2



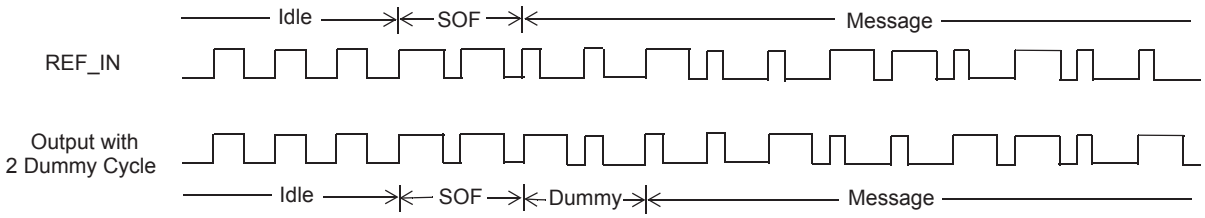
Message Forwarding from Output Clocks (OUT1 - OUT12) with PWM

Each or all of twelve LVDS output clocks can carry a message via PWM to the receiving side. Each output can carry a different message. The message source for each output can be from either de-modulating a message that had been modulated onto the input reference clock (REF_IN) or written directly from user generated and supplied data that is updated periodically.

If the output message source is selected to come from a de-modulated message on the reference clock input (REF_IN), there is a requirement for dummy cycles to be inserted between the SOF and the message. This is shown in Fig 3. The number of dummy cycles created is programmable from 2 to 8. The duty cycle of each dummy cycle is also programmable.

REF_IN to Output PWM Forward

Figure 3



When the message is taken from user supplied data, the modulation format is programmable. Message zero or one can be defined as 25% or 75% high of one clock cycle. 50% high time is reserved for “idle” cycle. Each bit can be either modulated by one clock cycle or two clock cycles. If the message is modulated by two clock cycles, the sum of these two clock cycle’s high time will be 50% of two clock periods. The bit transmitted sequence within a byte can be either LSB or MSB.

When the output message comes from user supplied data, the data is updated periodically in each frame. Messages written in the Nth frame period will be sent out in the (N+1)th frame period. The number of bytes to be sent in the (N+1)th frame period is determined by the number of bytes written into the buffer during Nth frame period. After the number of programmed bytes is sent, the rest of the clock cycles in the frame will be 50% duty clock cycle. Each output port has an individual double-buffer for the user message, so the output message can be different for each output. The user can update one buffer while the other buffer is transmitting. The data can also be read back for checking. If the message for all outputs are the same, there is a global update mechanism so the user does not need to write the same data to each of the 12 output ports individually.

NTC1012 General Description continued

Frequency Offset Calculation Between FRAME_IN and Inputs (IN1 - IN12)

The NTC1012 allows the user to calculate the fractional frequency offset between a selected (programmable) clock input and the given framing reference (FRAME_IN). The input to be checked must be 8kHz clock. The frequency offset checking period is programmable in 1, 2, 4 or 8 seconds. When the checking period is complete, NTC1012 will assert one of event status and report the frequency offset in 10 ppb unit.

1. Calculates the fractional frequency offset of one (programmable) of the 12 clock inputs (IN1~IN12).
2. Programmable observation period of 1/2/4/8 seconds
3. Fractional frequency offset will be calculated as the phase drifted over the observation period.
4. Fractional frequency offset difference measurement is provided in 10ppb units.
5. An interrupt will be trigged to inform the readiness of the fractional frequency offset result.

Phase Delay Measurement from FRAME_IN to Inputs (IN1 - IN12)

NTC1012 can measure the phase delay from FRAME_IN to the inputs. The measurement can be done with one input at a time. The input to be measured must be the same frequency as FRAME_IN. The number of measurements is programmable in 1, 2, 4, 8 or 16 times. When the measurement is complete, NTC1012 will assert one of the event status register and report each measurement and the average in ps unit.

The NTC1012 allows the user to measure the phase difference between a selected (programmable) clock input and the given framing reference (FRAME_IN).

1. Measures the phase difference between one (programmable) of the 12 clock inputs (IN1~IN12) versus the framing reference (FRAME_IN)
2. Averages and stores the phase differences of multiple successive measurements
3. Programmable number (1/2/4/8/16) of successive measurements to be average and stored
4. Phase difference measurement is provided in ps units.
5. An interrupt will be trigged to inform the readiness of the phase measurement results and their average value

Outputs from Selected Inputs (IN1 - IN12)

The NTC1012 allows the user to generate two single ended bypass outputs to assist in the frequency and phase measurement process. The two selected inputs can be selected through register programming from any of the up to 12 LVDS clock inputs (IN1~IN12) it receives. The two selected clock inputs are then bypassed through the IC and output as single-ended 3.3V LVCMOS signals the same frequency at pins (IN_SEL_OUT1) and (IN_SEL_OUT2).

NTC1012 Serial Interface

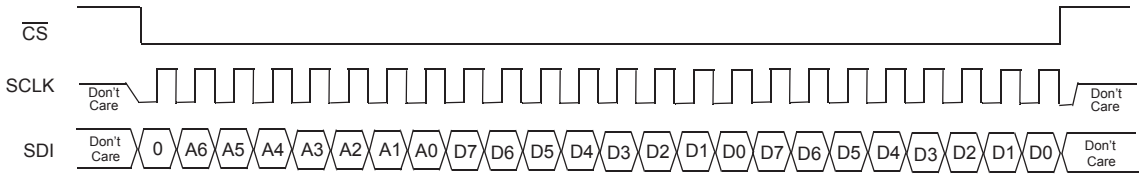
The NTC1012 supports both SPI or I2C serial interfaces for the user to communicate with the IC. The user can select which method they would like to interface with the IC by setting the pin BUS_TYPE to the appropriate logic level to select the bus type. When BUS_TYPE pin is set high, SPI is active, otherwise I2C is active by default

SPI Mode Operation

In SPI mode, single or multiple byte transfers are supported. The address and data bytes are sent in MSB first. A write or a read operation to the NTC1012 is initiated by pulling CS low. Bit 7 of first byte indicates the operation type, bit 6 - 0 of first byte indicates the address of first byte of data. For multiple byte access, the internal address will keep increment by one for each byte access. Fig 4 shows the write operation.

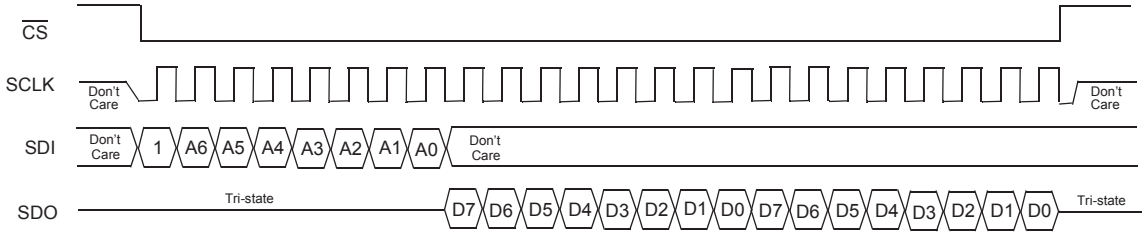
SPI Write Operation

Figure 4



SPI Read Operation

Figure 5

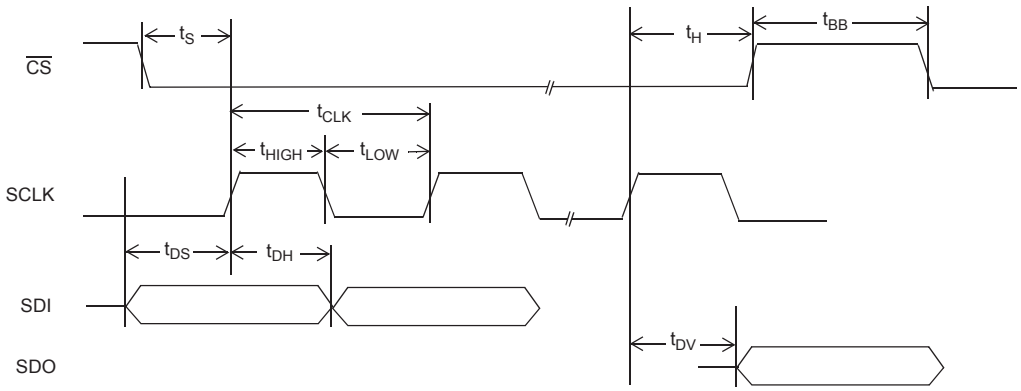


NTC1012 Serial Interface continued

SPI timing symbols are shown in Fig 6, and timing parameters are shown in Table 1.

SPI Timing Symbols

Figure 6



SPI Timing Parameters

Table 1

Parameters	Description	Min	Typ	Max	Unit
t_{CLK}	Period of SCLK	40	-	-	ns
t_{HIGH}	SCLK high time	15	-	-	ns
t_{LOW}	SCLK low time	15	-	-	ns
t_S	Setup time between CS to SCLK rising edge for initiating the transmission	10	-	-	ns
t_H	Hold time between CS to SCLK rising edge for ending the transmission	12	-	-	ns
t_{DS}	Setup time between SDI and SCLK rising edge	10	-	-	ns
t_{DH}	Hold time between SDI and SCLK rising edge	7	-	-	ns
t_{DV}	SCLK to SDO data valid time	-	-	20	ns
t_{BB}	Minimum gap for back to back transmission	20	-	-	ns

Recommended Operating Conditions

Table 2

Parameters		Symbol	Min	Typ	Max	Unit
Ambient Temperature	TA	-40		25 85	°C	
Junction Temperature	TJ_{MAX}	-	-	125	°C	
Digital Core Supply Voltage		DVDD18	1.70	1.80	1.90	V
Digital IO Supply Voltage		DVDD33	3.00	3.30	3.60	V
PLL Power Supply	VDD33_PLL	3.15		3.30 3.45	V	
Power Supply for Internal LDO for PLL Feedback Circuit	VDD33_FB	3.15		3.30 3.45	V	
Power Supply for Internal LDO and LOOP_OUT and OUT1 - OUT12 Transmitter		VDD33_TX	3.15	3.30	3.45	V
Power Supply for Internal LDO and REFD, LOOP_IN and IN1 - IN12 Receiver		VDD33_RX	3.15	3.30	3.45	V

DC Characteristics

Table 3

Parameters	Symbol	Typ	Max	Unit
Digital Core Supply Current	I_{DVDD18}	60	57	mA
Digital IO Supply Current	I_{DVDD33}	2	3	mA
PLL Supply Current	I_{VDD33_PLL}	35	39	mA
Power Supply Current for Internal LDO for PLL Feedback Circuit	I_{VDD33_FB}	49	54	mA
Power Supply Current for Internal LDO and OUT1 - OUT12 Transmitter	I_{VDD33_TX}	262	290	mA
Power Supply Current for Internal LDO and REFS, REFD, LOOP_IN and IN1 - IN12 Receiver	I_{VDD33_RX}	168	186	mA

LVDS Input Specification

Table 4

Parameters		Min	Typ	Max	Unit
Input Common Mode Voltage	0	-	1.73	V	
Input Differential Mode Voltage		100	-	800	mV
Maximum Input Voltage		-	-	5.5	V
Capacitance		-	0.4	-	pF

FRAME_IN Specification

Table 5

Parameters	Min	Typ	Max	Unit
LVCMOS Input Voltage	-0.3	-	3.6	V
Input Low Voltage	-	-	1.823	V
Input High Voltage	1.425	-	-	V
Maximum Input Voltage	-	-	5.5	V
Input Leakage Current	-	-	±1	uA
Capacitance	-	0.4	-	pF

Electrical Specification continued

LVCMOS Input Specification

Table 6

Parameters	Min	Typ	Max	Unit
LVCMOS Input Voltage	-0.3	-	3.6	V
Input Low Voltage	-0.3	-	0.8	V
Input High Voltage	2	-	3.6	V
Maximum Input Voltage	-	-	5.5	V
Input Leakage Current	-	-	±1	uA
Capacitance	-	2.6647	-	pF

LVDS Output Specification

Table 7

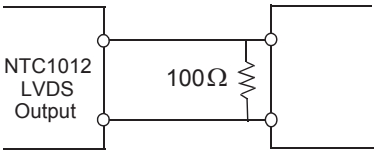
Parameters	Min	Typ	Max	Unit	Note
Output Common Mode Voltage	1.748	1.974	2.173	V	
Output Differential Mode Voltage	635	703	784	mV	
Rise and Fall Time (20% - 80%)	88.4/125	99.3/121	155/135	pS	1pF C-Load

LVCMOS Output Specification

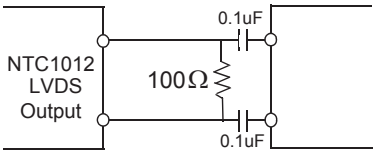
Table 8

Parameters	Min	Typ	Max	Unit
LVCMOS Output Voltage	0	-	3.6	V
Output Low Voltage	-	-	0.4	V
Output High Voltage	2.4	-	-	V
Output Low Current	11.5	17.6	23.2	mA
Output High Current	12.7	25.6	42.5	mA

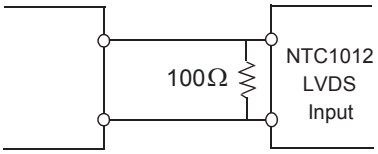
Input Output Termination Recommendations



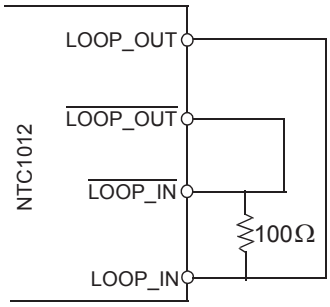
DC Coupled LVDS Output



AC Coupled LVDS Output



DC Coupled LVDS Input

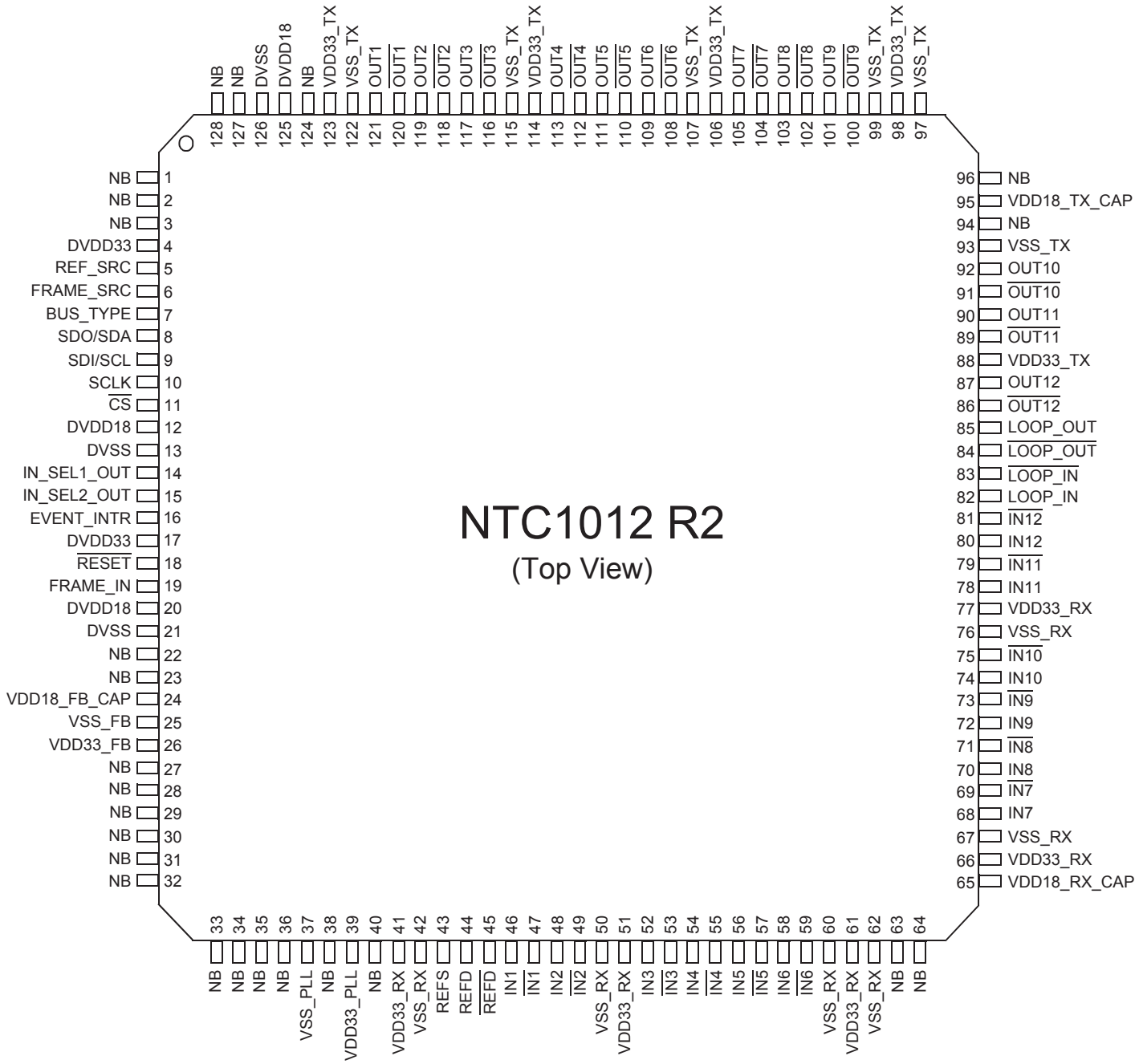


DC Coupled Loop Back Connection

Pin Diagram

NTC1012 Pin Description

Figure 6



Pin Descriptions

Pin#	Name	Type	IO	Description
5	REF_SRC	LVCMOS	I	Select reference source, 0: REFS, 1: REFD/$\overline{\text{REFD}}$
6	FRAME_SRC	LVCMOS	I	Select frame input source, 0: FRAME_IN, 1: reference PWM data
7	BUS_TYPE	LVCMOS	I	Select bus mode, 0: I2C, 1: SPI
8	SDO/SDA	LVCMOS	IO	SDO pin when bus mode is SPI, SDA pin when bus mode is I2C
9	SDI/SCL	LVCMOS	I	SDI pin when bus mode is SPI, SCL pin when bus mode is I2C
10	SCLK	LVCMOS	I	CLK pin when SPI bus mode is used
11	$\overline{\text{CS}}$	LVCMOS	I	Chip select pin when SPI bus mode is used
14	IN_SEL1_OUT	LVCMOS	O	Selected output from IN1 - IN12
15	IN_SEL2_OUT	LVCMOS	O	Selected output from IN1 - IN12
16	EVENT_INTR	LVCMOS	O	Assert high to notify pre-defined events
18	$\overline{\text{RESET}}$	LVCMOS	I	Assert low to reset IC, minimal low pulse is 1us
19	FRAME_IN	LVCMOS	I	100Hz - 8kHz frame input signal
43	REFS	LVCMOS	I	25MHz single-ended reference clock with optional PWM message
44	REFD	LVDS	I	Along with $\overline{\text{REFD}}$, it is LVDS differential input for 25MHz reference clock with optional PWM message
45	$\overline{\text{REFD}}$	LVDS	I	Complemental input signal of REFD
46	IN1	LVDS	I	Along with $\overline{\text{IN1}}$, it is LVDS differential input from 100Hz - 8kHz signal
47	$\overline{\text{IN1}}$	LVDS	I	Complemental input signal of IN1
48	IN2	LVDS	I	Along with $\overline{\text{IN2}}$, it is LVDS differential input from 100Hz - 8kHz signal
49	$\overline{\text{IN2}}$	LVDS	I	Complemental input signal of IN2
52	IN3	LVDS	I	Along with $\overline{\text{IN3}}$, it is LVDS differential input from 100Hz - 8kHz signal
53	$\overline{\text{IN3}}$	LVDS	I	Complemental input signal of IN3
54	IN4	LVDS	I	Along with $\overline{\text{IN4}}$, it is LVDS differential input from 100Hz - 8kHz signal
55	$\overline{\text{IN4}}$	LVDS	I	Complemental input signal of IN4
56	IN5	LVDS	I	Along with $\overline{\text{IN5}}$, it is LVDS differential input from 100Hz - 8kHz signal
57	$\overline{\text{IN5}}$	LVDS	I	Complemental input signal of IN5
58	IN6	LVDS	I	Along with $\overline{\text{IN6}}$, it is LVDS differential input from 100Hz - 8kHz signal
59	$\overline{\text{IN6}}$	LVDS	I	Complemental input signal of IN6
68	IN7	LVDS	I	Along with $\overline{\text{IN7}}$, it is LVDS differential input from 100Hz - 8kHz signal
69	$\overline{\text{IN7}}$	LVDS	I	Complemental input signal of IN7
70	IN8	LVDS	I	Along with $\overline{\text{IN8}}$, it is LVDS differential input from 100Hz - 8kHz signal
71	$\overline{\text{IN8}}$	LVDS	I	Complemental input signal of IN8
72	IN9	LVDS	I	Along with $\overline{\text{IN9}}$, it is LVDS differential input from 100Hz - 8kHz signal
73	$\overline{\text{IN9}}$	LVDS	I	Complemental input signal of IN9
74	IN10	LVDS	I	Along with $\overline{\text{IN10}}$, it is LVDS differential input from 100Hz - 8kHz signall
75	$\overline{\text{IN10}}$	LVDS	I	Complemental input signal of IN10
78	IN11	LVDS	I	Along with $\overline{\text{IN11}}$, it is LVDS differential input from 100Hz - 8kHz signal
79	$\overline{\text{IN11}}$	LVDS	I	Complemental input signal of IN11
80	IN12	LVDS	I	Along with $\overline{\text{IN12}}$, it is LVDS differential input from 100Hz - 8kHz signal
81	$\overline{\text{IN12}}$	LVDS	I	Complemental input signal of IN12
82	LOOP_IN	LVDS	I	Along with $\overline{\text{LOOP\_IN}}$, it is LVDS differential input for loop back signal
83	$\overline{\text{LOOP\_IN}}$	LVDS	I	Complemental input signal of LOOP_IN
84	LOOP_OUT	LVDS	I	Complement output signal of LOOP_OUT
85	LOOP_OUT	LVDS	I	Along with $\overline{\text{LOOP\_OUT}}$, it is LVDS differential output for loop back signal
86	$\overline{\text{OUT12}}$	LVDS	I	Complemental output signal of OUT12
87	OUT12	LVDS	I	Along with $\overline{\text{OUT12}}$, it is 25MHz LVDS differential output with PWM message
89	$\overline{\text{OUT11}}$	LVDS	I	Complemental output signal of OUT11
90	OUT11	LVDS	I	Along with $\overline{\text{OUT11}}$, it is 25MHz LVDS differential output with PWM message
91	$\overline{\text{OUT10}}$	LVDS	I	Complemental output signal of OUT10
92	OUT10	LVDS	I	Along with $\overline{\text{OUT10}}$, it is 25MHz LVDS differential output with PWM message
100	$\overline{\text{OUT9}}$	LVDS	I	Complemental output signal of OUT9

Pin Descriptions continued

Pin#	Name	Type	IO	Description
101	OUT9	LVDS	I	Along with $\overline{OUT9}$, it is 25MHz LVDS differential output with PWM message
102	$\overline{OUT8}$	LVDS	I	Complemental output signal of OUT8
103	OUT8	LVDS	I	Along with $\overline{OUT8}$, it is 25MHz LVDS differential output with PWM message
104	$\overline{OUT7}$	LVDS	I	Complemental output signal of OUT7
105	OUT7	LVDS	I	Along with $\overline{OUT7}$, it is 25MHz LVDS differential output with PWM message
108	$\overline{OUT6}$	LVDS	I	Complemental output signal of OUT6
109	OUT6	LVDS	I	Along with $\overline{OUT6}$, it is 25MHz LVDS differential output with PWM message
110	$\overline{OUT5}$	LVDS	I	Complemental output signal of OUT5
111	OUT5	LVDS	I	Along with $\overline{OUT5}$, it is 25MHz LVDS differential output with PWM message
112	$\overline{OUT4}$	LVDS	I	Complemental output signal of OUT4
113	OUT4	LVDS	I	Along with $\overline{OUT4}$, it is 25MHz LVDS differential output with PWM message
116	$\overline{OUT3}$	LVDS	I	Complemental output signal of OUT3
117	OUT3	LVDS	I	Along with $\overline{OUT3}$, it is 25MHz LVDS differential output with PWM message
118	$\overline{OUT2}$	LVDS	I	Complemental output signal of OUT2
119	OUT2	LVDS	I	Along with $\overline{OUT2}$, it is 25MHz LVDS differential output with PWM message
120	$\overline{OUT1}$	LVDS	I	Complemental output signal of OUT1
121	OUT1	LVDS	I	Along with $\overline{OUT1}$, it is 25MHz LVDS differential output with PWM message
4 17	DVDD33	Power	P	3.3V supply for digital IO
12 20 125	DVDD18	Power	P	1.8V supply for digital core
13 21 126	DVSS	Ground	GND	Digital ground
24	VDD18_FB_CAP	Power Output	P/O	1.8 V internal LDO regulator de-coupling pin. Connect a 1µF decoupling capacitor from this pin to ground.
25	VSS_FB	Ground	GND	Ground for internal PLL feedback circuit
26	VDD33_FB	Power	P	3.3V supply for Internal PLL feedback circuit LDO
37	VSS_PLL	Ground	GND	Ground for PLL
39	VDD33_PLL	Power	P	3.3V supply for PLL
41 51 61 66 77	VDD33_RX	Power	P	3.3V supply for internal LDO and REFS, REFD, LOOP_IN, and IN1 - IN12 receivers
42 50 60 62 67 76	VSS_RX	Ground	GND	Ground for REFS, REFD, LOOP_IN, and IN1 - IN12 receivers
65	VDD18_RX_CAP	Power Output	P	Internal LDO 1.8V output pin for regulator de-coupling. Connect a 1µF de-coupling capacitor from this pin to ground
88 98 106 114 123	VDD33_TX	Power	P	3.3V supply for internal LDO and LOOP_OUT and OUT1 - OUT12 transmitter
93 97 99 107 115 122	VSS_TX	Ground	GND	Ground for LOOP_OUT and OUT1 - OUT12 transmitter
95	VDD18_TX_CAP	Power Output	P/O	Internal LDO 1.8V output pin for regulator de-coupling. Connect a 1µF de-coupling capacitor from this pin to ground

Pin Descriptions continued

Pin#	Name	Type	IO	Description
1	NB			Not Internally Bonded
2				
3				
22				
23				
27				
28				
29				
30				
31				
32				
33				
34				
35				
36				
38				
40				
63				
64				
94				
96				
124				
127				
128				

Register Table

Addr	Name	Type	Bits	Default	Description
0x00 - 0x01	Chip ID	R	15 - 0	0x1012	Chip ID
0x02	Chip Revision	R	7 - 0	2	Chip revision
0x03	Reserved				
0x04 - 0x07	Frame Size	RW	24 - 0	25000	Frame size in number of cycle of 25Mhz clock
0x08	Minimum Idle Cycle	RW	7 - 0	100	Minimum idle cycle between PWM data and next SYNC Cycle
0x09	Reference Parameters	RW	5 - 0	0x24	[3:0] Reserved [5:4] # of SOF cycle, 0 or 1: 1, 2: 2, 3: 3
0x0a	Dummy Cycle	RW	3 - 0	2	Number of dummy cycles inserted when PWM generator take the PWM message from reference.If the value < 2, it will be treated as 2. If the value > 8, it will be treated as 8.
0x0b - 0x0c	PWM Dummy Cycle Content	RW	15 - 0	0x5555	The dummy cycle content. Every 2 bits are associated with one dummy cycle the encode scheme as follows. 00: 25%, 01: 75%, 10: 50%, 11: don't use The sequence of associated bits are as follows, Bit[1:0] -> 1st dummy bit Bit[3:2] -> 2nd dummy bit Bit[5:4] -> 3rd dummy bit Bit[7:6] -> 4th dummy bit Bit[9:8] -> 5th dummy bit Bit[11:10] -> 6th dummy bit Bit[13:12] -> 7th dummy bit Bit[15:14] -> 8th dummy bit
0x0d	Start/Restart PLL	RW	0	0	The value change from 0 to 1 will trig PLL to re-lock the reference and re-search frame SYNC position
0x0e	PLL Status	R	3 - 0	0	PLL status indication, [0] reference lock indication, 0: not locked 1: locked [1] frame sync position status, 0: not located, 1: located [2] frame sync los indication, 0: no los, 1: los [3] frame sync position error, 0: no error, 1: inconsistent frame sync position
0x0f	Event Status	RW	5 - 0	0	6 different event status, if the associated status changed, the bit will be changed to 1 until the user write 1 to clear this bit, [0] reference lock indication changed [1] frame sync position status changed [2] frame sync los indication changed [3] frame sync position error status changed [4] phase delay calculation command is complete [5] frequency offset calculation command is complete
0x10 - 0x11	Phase Skew Control	RW	12 - 0	0	Skew adjustment between SYNC edge and OUTx. It is a 2's complement value in ps unit. Positive value makes positive delay for OUTx, negative value makes negative delay for OUTx
0x12	Reserved				
0x13	OUT1 Parameter	RW	7 - 0	0x08	[3:0] is reserved [4] PWM data source, 0: user supply, 1: from reference [5] If PWM data is from user, this bit define the output PWM cycle per bit, 0: 1 cycle per bit, 1: two cycle per bit [6] If PWM data is from user, this bit select the LSB or MSB of transmission order in each byte, 0: LSB, 1: MSB [7] Transmitter on or off, 0: power down transmitter, 1: power up transmitter
0x14	Reserved				

Register Table continued

Addr	Name	Type	Bits	Default	Description
0x15	OUT2 Parameter	RW	7 - 0	0x08	[3:0] is reserved [4] PWM data source, 0: user supply, 1: from reference [5] If PWM data is from user, this bit define the output PWM cycle per bit, 0: 1 cycle per bit, 1: two cycle per bit [6] If PWM data is from user, this bit select the LSB or MSB of transmission order in each byte, 0: LSB, 1: MSB [7] Transmitter on or off, 0: power down transmitter, 1: power up transmitter
0x16	Reserved				
0x17	OUT3 Parameter	RW	7 - 0	0x08	[3:0] is reserved [4] PWM data source, 0: user supply, 1: from reference [5] If PWM data is from user, this bit define the output PWM cycle per bit, 0: 1 cycle per bit, 1: two cycle per bit [6] If PWM data is from user, this bit select the LSB or MSB of transmission order in each byte, 0: LSB, 1: MSB [7] Transmitter on or off, 0: power down transmitter, 1: power up transmitter
0x18	Reserved				
0x19	OUT4 Parameter	RW	7 - 0	0x08	[3:0] is reserved [4] PWM data source, 0: user supply, 1: from reference 5] If PWM data is from user, this bit define the output PWM cycle per bit, 0: 1 cycle per bit, 1: two cycle per bit [6] If PWM data is from user, this bit select the LSB or MSB of transmission order in each byte, 0: LSB, 1: MSB [7] Transmitter on or off, 0: power down transmitter, 1: power up transmitter
0x1a	Reserved				
0x1b	OUT5 Parameter	RW	7 - 0	0x08	[3:0] is reserved [4] PWM data source, 0: user supply, 1: from reference [5] If PWM data is from user, this bit define the output PWM cycle per bit, 0: 1 cycle per bit, 1: two cycle per bit [6] If PWM data is from user, this bit select the LSB or MSB of transmission order in each byte, 0: LSB, 1: MSB [7] Transmitter on or off, 0: power down transmitter, 1: power up transmitter
0x1c	Reserved				
0x1d	OUT6 Parameter	RW	7 - 0	0x08	[3:0] is reserved [4] PWM data source, 0: user supply, 1: from reference [5] If PWM data is from user, this bit define the output PWM cycle per bit, 0: 1 cycle per bit, 1: two cycle per bit [6] If PWM data is from user, this bit select the LSB or MSB of transmission order in each byte, 0: LSB, 1: MSB [7] Transmitter on or off, 0: power down transmitter, 1: power up transmitter
0x1e	Reserved				
0x1f	OUT7 Parameter	RW	7 - 0	0x08	[3:0] is reserved [4] PWM data source, 0: user supply, 1: from reference [5] If PWM data is from user, this bit define the output PWM cycle per bit, 0: 1 cycle per bit, 1: two cycle per bit [6] If PWM data is from user, this bit select the LSB or MSB of transmission order in each byte, 0: LSB, 1: MSB [7] Transmitter on or off, 0: power down transmitter, 1: power up transmitter
0x20	Reserved				

Register Table continued

Addr	Name	Type	Bits	Default	Description
0x21	OUT8 Parameter	RW	7 - 0	0x08	[3:0] is reserved [4] PWM data source, 0: user supply, 1: from reference [5] If PWM data is from user, this bit define the output PWM cycle per bit, 0: 1 cycle per bit, 1: two cycle per bit [6] If PWM data is from user, this bit select the LSB or MSB of transmission order in each byte, 0: LSB, 1: MSB [7] Transmitter on or off, 0: power down transmitter, 1: power up transmitter
0x22	Reserved				
0x23	OUT9 Parameter	RW	7 - 0	0x08	[3:0] is reserved [4] PWM data source, 0: user supply, 1: from reference [5] If PWM data is from user, this bit define the output PWM cycle per bit, 0: 1 cycle per bit, 1: two cycle per bit [6] If PWM data is from user, this bit select the LSB or MSB of transmission order in each byte, 0: LSB, 1: MSB [7] Transmitter on or off, 0: power down transmitter, 1: power up transmitter
0x24	Reserved				
0x25	OUT10 Parameter	RW	7 - 0	0x08	[3:0] is reserved [4] PWM data source, 0: user supply, 1: from reference [5] If PWM data is from user, this bit define the output PWM cycle per bit, 0: 1 cycle per bit, 1: two cycle per bit [6] If PWM data is from user, this bit select the LSB or MSB of transmission order in each byte, 0: LSB, 1: MSB [7] Transmitter on or off, 0: power down transmitter, 1: power up transmitter
0x26	Reserved				
0x27	OUT11 Parameter	RW	7 - 0	0x08	[3:0] is reserved [4] PWM data source, 0: user supply, 1: from reference [5] If PWM data is from user, this bit define the output PWM cycle per bit, 0: 1 cycle per bit, 1: two cycle per bit [6] If PWM data is from user, this bit select the LSB or MSB of transmission order in each byte, 0: LSB, 1: MSB [7] Transmitter on or off, 0: power down transmitter, 1: power up transmitter
0x28	Reserved				
0x29	OUT12 Parameter	RW	7 - 0	0x08	[3:0] is reserved [4] PWM data source, 0: user supply, 1: from reference [5] If PWM data is from user, this bit define the output PWM cycle per bit, 0: 1 cycle per bit, 1: two cycle per bit [6] If PWM data is from user, this bit select the LSB or MSB of transmission order in each byte, 0: LSB, 1: MSB [7] Transmitter on or off, 0: power down transmitter, 1: power up transmitter
0x2a	OUT1 FIFO data port	RW	7 - 0		The data port for fifo dedicated for OUT1
0x2b	OUT2 FIFO data port	RW	7 - 0		The data port for fifo dedicated for OUT2
0x2c	OUT3 FIFO data port	RW	7 - 0		The data port for fifo dedicated for OUT3
0x2d	OUT4 FIFO data port	RW	7 - 0		The data port for fifo dedicated for OUT4
0x2e	OUT5 FIFOt data port	RW	7 - 0		The data port for fifo dedicated for OUT5
0x2f	OUT6 FIFO data port	RW	7 - 0		The data port for fifo dedicated for OUT6

Register Table continued

Addr	Name	Type	Bits	Default	Description
0x30	OUT7 FIFO data port	RW	7 - 0		The data port for fifo dedicated for OUT7
0x31	OUT8 FIFO data port	RW	7 - 0		The data port for fifo dedicated for OUT8
0x32	OUT9 FIFO Data Port	RW	7 - 0		The data port for fifo dedicated for OUT9
0x33	OUT10 FIFO data port	RW	7 - 0		The data port for fifo dedicated for OUT10
0x34	OUT11 FIFO data port	RW	7 - 0		The data port for fifo dedicated for OUT11
0x35	OUT12 FIFO data port	RW	7 - 0		The data port for fifo dedicated for OUT12
0x36	Global FIFO data port	RW	7 - 0		The data port for global fifo, when write to this port, all FIFO will be updated, when read, the return value is OUT1 FIFO data
0x37	FIFO read/write pointer reset	RW	7 - 0	0x00	To reset one or all OUTs FIFO read/write pointer is to write to this port with data bits [7:5] == 3'b000, [3:0] select which OUT FIFO pointer to reset, 0: reset all FIFO, 1 to 12 is for OUT1 to OUT12 FIFO 13 to 15 will be no effect [4] select read or write pointer to reset 0: read pointer, 1: write pointer
0x38	IN_SEL1_OUT Source	RW	3 - 0	0	Select the source for IN_SEL1_OUT, 1: IN1, 2: IN2, 3: IN3, 4: IN4, 5: IN5, 6: IN6, 7: IN7, 8: IN8, 9: IN9, 10: IN10, 11: IN11, 12: IN12, 0, 13, 14, or 15: 0
0x39	IN_SEL2_OUT Source	RW	3 - 0	0	Select the source for IN_SEL2_OUT, 1: IN1, 2: IN2, 3: IN3, 4: IN4, 5: IN5, 6: IN6, 7: IN7, 8: IN8, 9: IN9, 10: IN10, 11: IN11, 12: IN12, 0, 13, 14, or 15: 0

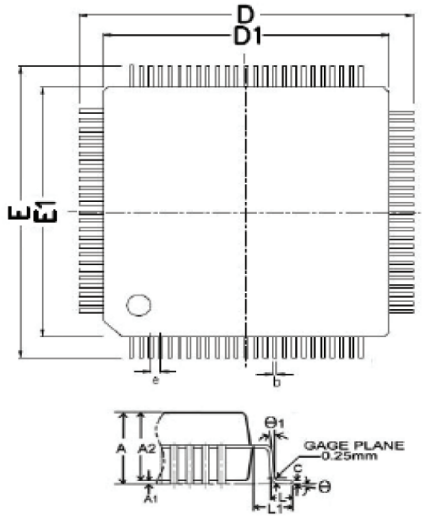
Register Table continued

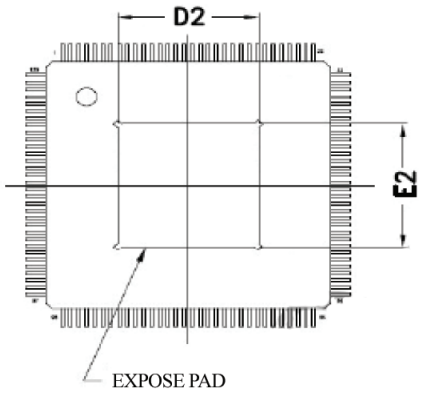
Addr	Name	Type	Bits	Default	Description
0x3a	Frequency Off-set Calculation Target	RW	3 - 0	0	Select the target for frequency offset calculation, 1: IN1, 2: IN2, 3: IN3, 4: IN4, 5: IN5, 6: IN6, 7: IN7, 8: IN8, 9: IN9, 10: IN10, 11: IN11, 12: IN12, 0,13, 14 or 15 are reserved
0x3b	Frequency Off-set Calculation Timer Selection	RW	1 - 0	0	Select the offset calculation time, 0: 1 sec, 1: 2 sec, 2: 4 sec, 3: 8 sec
0x3c	Frequency Off-set Calculation Command	RW	0	0	Write 1 to start frequency offset calculation, the value will be cleared to 0 when calculation is done, Reg 0x3a and 0x3b should be set to appropriate value before starting the frequency offset calculation
0x3d - 0x3e	Frequency Off-set Result	R	11 - 0	0	2's complement frequency offset value, the unit is 10 ppb
0x3f	Phase Delay Calculation Target	RW	3 - 0	0	Select the target for phase delay calculation, 1: IN1, 2: IN2, 3: IN3, 4: IN4, 5: IN5, 6: IN6, 7: IN7, 8: IN8, 9: IN9, 10: IN10, 11: IN11, 12: IN12, 0, 13, 14 or 15 are reserved
0x40	Phase Delay Calculation Time Selection	RW	3 - 0	0	Select how many times to compare the delay between FRAME_IN and the selected target, 0: 1, 1: 2, 2: 4, 3: 8, 4 ~ 7: 16
0x41	Phase Delay Calculation Command	RW	0	0	Write 1 to start phase delay calculation, the value will be cleared to 0 when calculation is done, Reg 0x3f and 0x40 should be set to appropriate value before starting the calculation
0x42 - 0x43	Average of Phase Delay	R	15 - 0	0	The average of phase delay calculation in ps unit
0x44 - 0x45	1st Phase Delay Value	R	15 - 0	0	1st calculated phase delay value in ps unit
0x46 - 0x47	2nd Phase Delay Value	R	15 - 0	0	2nd calculated phase delay value in ps unit

Register Table continued

Addr	Name	Type	Bits	Default	Description
0x48 - 0x49	3rd Phase Delay Value	R	15 - 0	0	3rd calculated phase delay value in ps unit
0x4a - 0x4b	4th Phase Delay Value	R	15 - 0	0	4th calculated phase delay value in ps unit
0x4c - 0x4d	5th Phase Delay Value	R	15 - 0	0	5th calculated phase delay value in ps unit
0x4e - 0x4f	6th Phase Delay Value	R	15 - 0	0	6th calculated phase delay value in ps unit
0x50 - 0x51	7th Phase Delay Value	R	15 - 0	0	7th calculated phase delay value in ps unit
0x52 - 0x53	8th Phase Delay Value	R	15 - 0	0	8th calculated phase delay value in ps unit
0x54 - 0x55	9th Phase Delay Value	R	15 - 0	0	9th calculated phase delay value in ps unit
0x56 - 0x57	10th Phase Delay Value	R	15 - 0	0	10th calculated phase delay value in ps unit
0x58 - 0x59	11th Phase Delay Value	R	15 - 0	0	11th calculated phase delay value in ps unit
0x5a - 0x5b	12th Phase Delay Value	R	15 - 0	0	12th calculated phase delay value in ps unit
0x5c - 0x5d	13th Phase Delay Value	R	15 - 0	0	13th calculated phase delay value in ps unit
0x5e - 0x5f	14th Phase Delay Value	R	15 - 0	0	14th calculated phase delay value in ps unit
0x60 - 0x61	15th Phase Delay Value	R	15 - 0	0	15th calculated phase delay value in ps unit
0x62 - 0x63	16th Phase Delay Value	R	15 - 0	0	16th calculated phase delay value in ps unit

NTC1012 Pin Package Outline and Dimensions



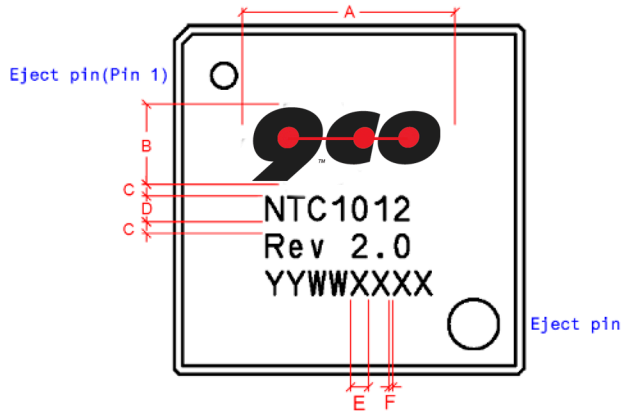


SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	—	0.23
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°
θ1	0°	—	—

PAD SIZE (MIL)	MILLIMETER		
	D2/E2		
	MIN.	NOM.	MAX.
273X273-A	6.855	—	7.055

NTC1012 Package Marking

TOP MARKING CONTENT



DIMENSION: Unit mm (Font Size +/-0.2mm)

A	B	C	D	E	F
8.50	3.20	0.50	1.00	0.70	0.15

Pin1 Location

	(V)	( )	( )	
	1	2	3	
( )	4	PGC	5	( )
	6	7	8	
	( )	( )	( )	

Marking Descriptions

	Content	Description	Fixed/Dynamic
Line 1	9co	Logo	Fixed
Line 2	NTC1012	Device Name	Fixed
Line 3	Rev 2.0	Assigned Rev Code	Fixed
Line 4	YYWWXXXX	Datecode: (YY= Year, WW=Week, XXXX=Serial Number	Dynamic

Revision History

Revision	Date	Note
00	01/06/2019	New Release

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